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MS-7B06

m-ATX

Ver: 12

Basinfall Platform

CPU:

Skylake X

System Chipset:

Kaby Lake PCH-X

Onboard Chip:

HD Audio Codec:ALC1220

LAN-Intel i219 , Intel i211

SIO:NTC6795D

Dual Flash ROM: SPI 64 MB X2

Main Memory:

DDRIV (UP to 2677MHz) * 8DIMM (4 Channel)

ACPI:

MPS

PWM:

VR13 -IR35201

Expansion Slots:

Other:

					44 lanes	28 lanes	
PCI_E1					X16	X16	M2 (2280) 位置在DIMM旁
PCI_E2					X16	X8	
PCI_E3					X8	X4	

SATA3.0 *8

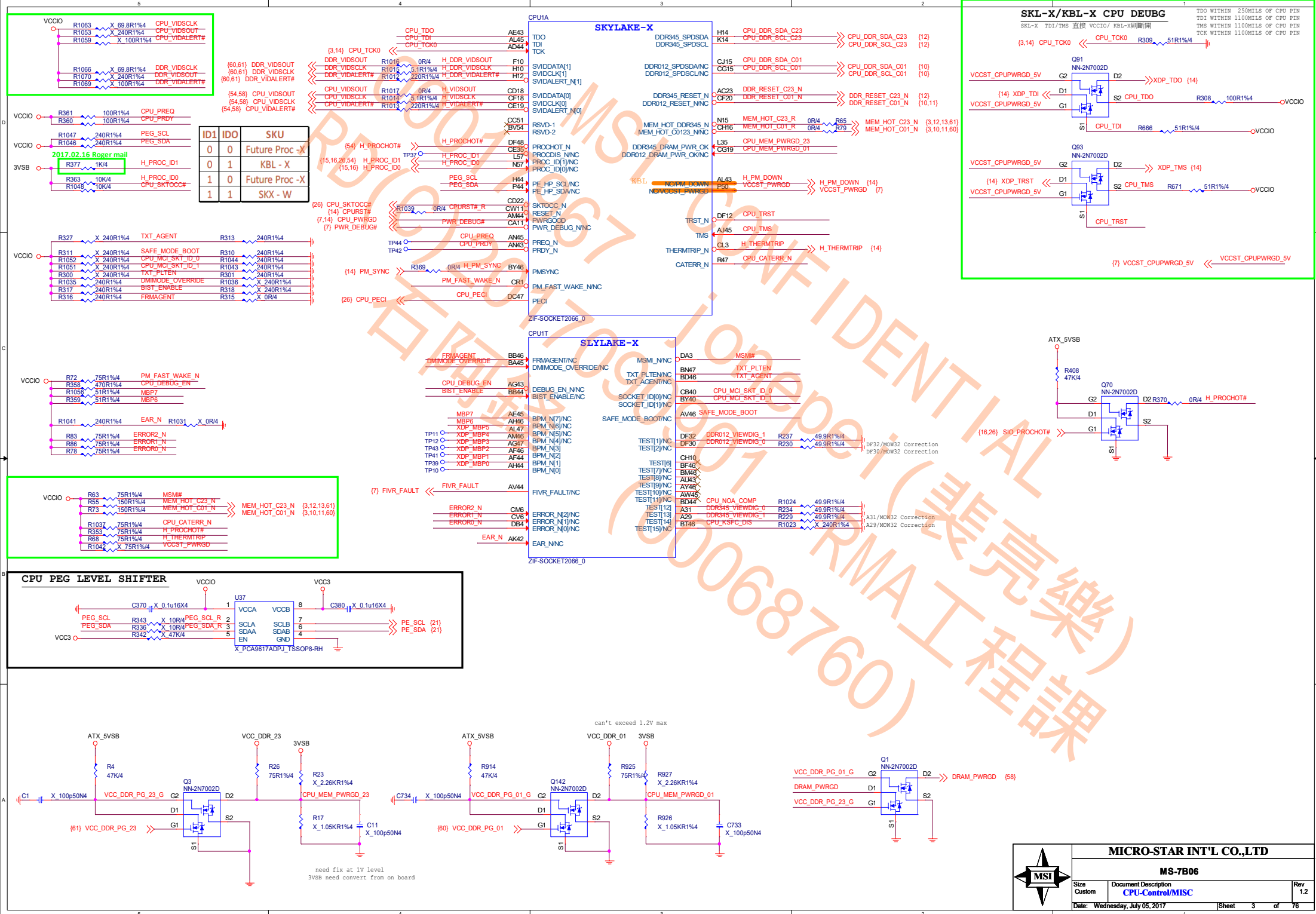
USB2.0 *8 Ports (2R/4F)

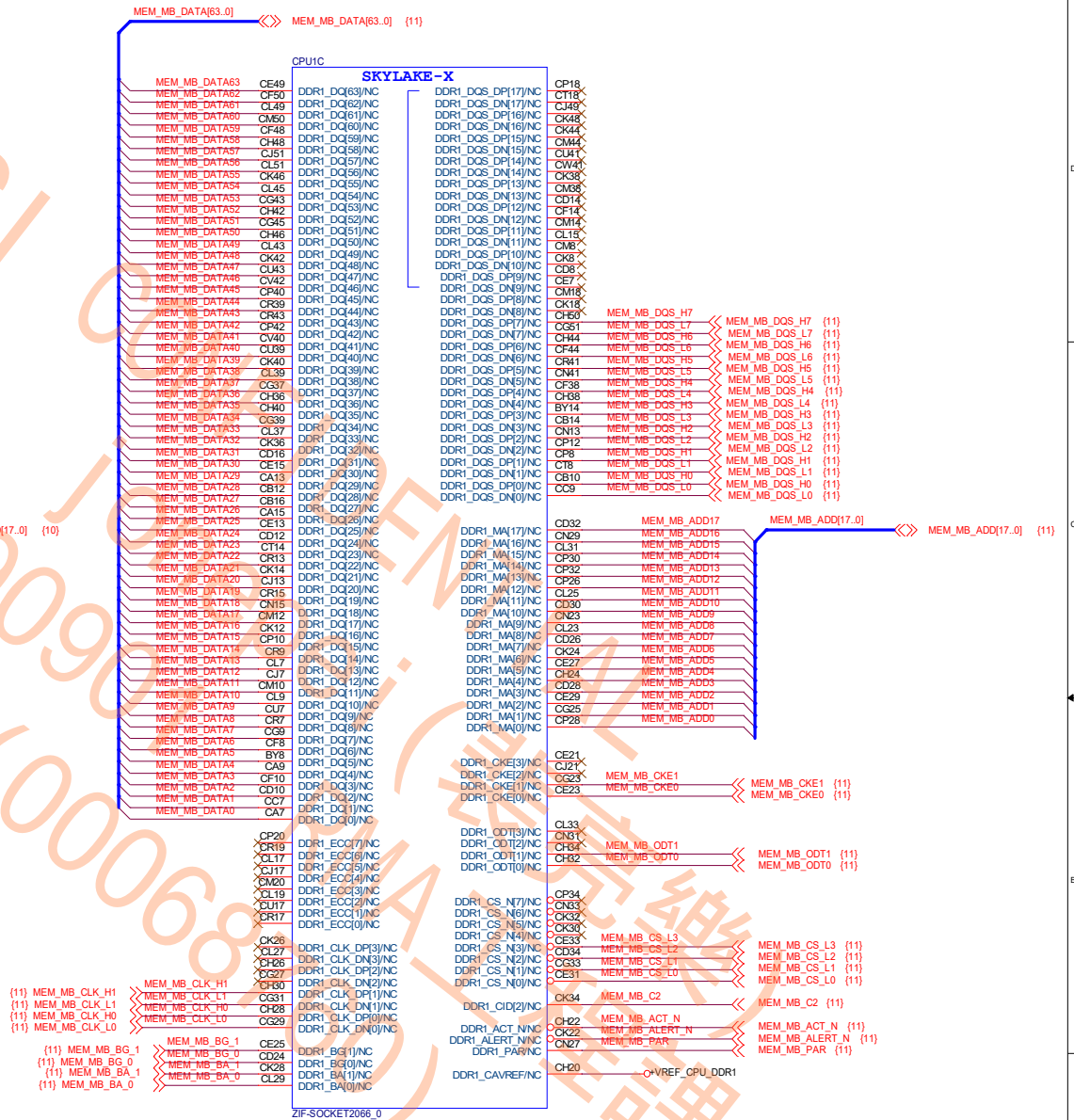
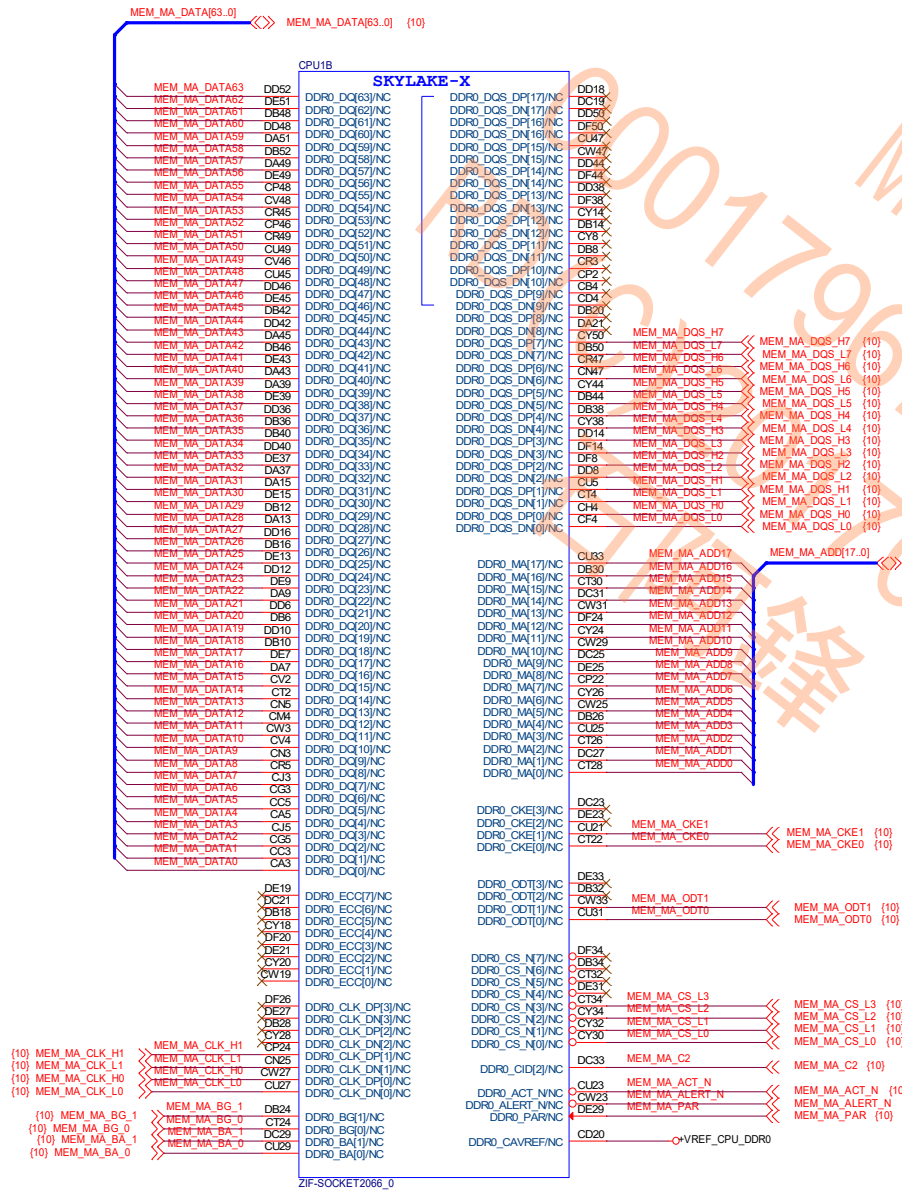
REAR USB30*4 + USB3.1*1 & TYPEC*1

FRONT USB3.0 *2+TYPEC*1

17ci203

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MS-7B06		
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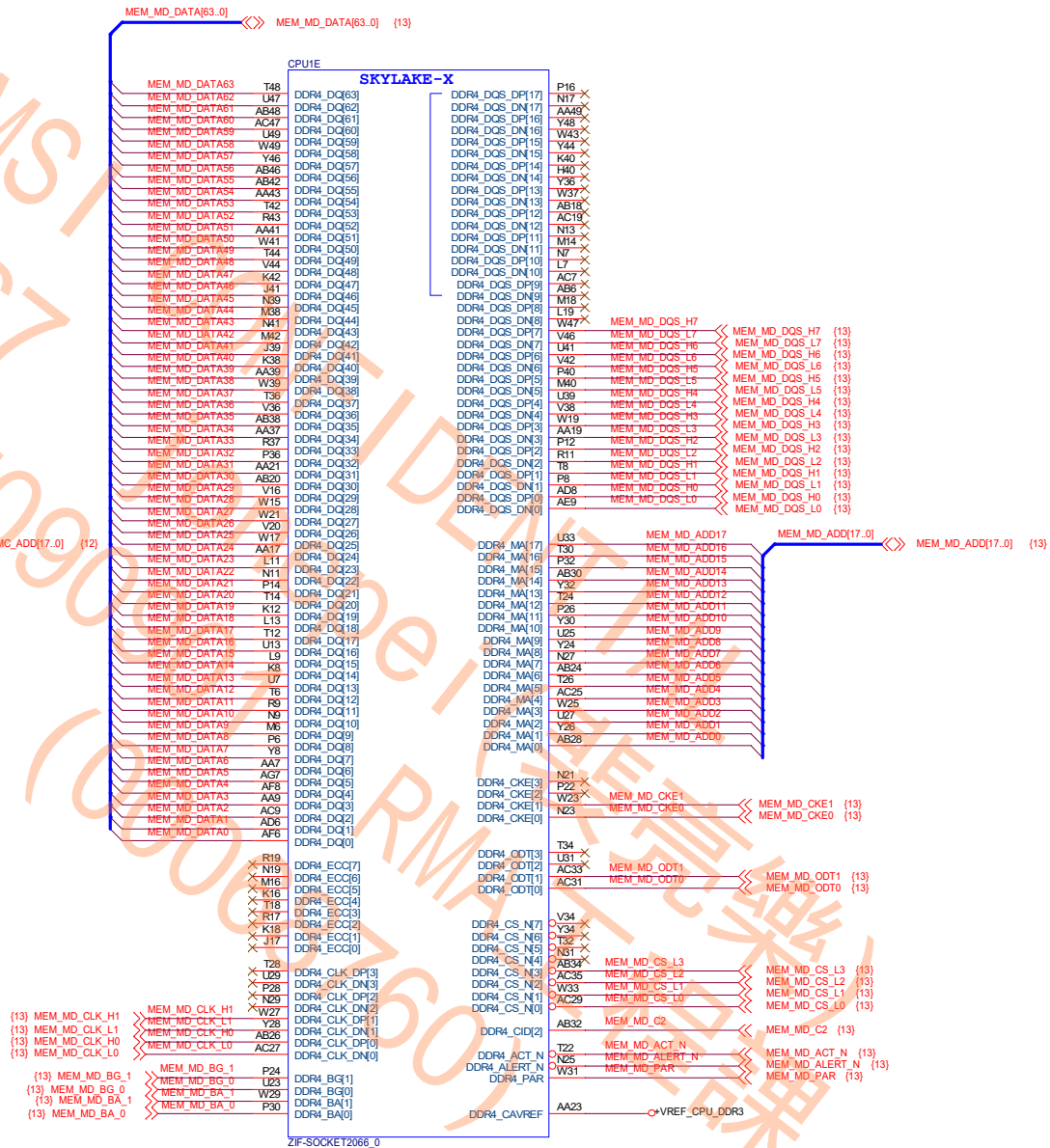
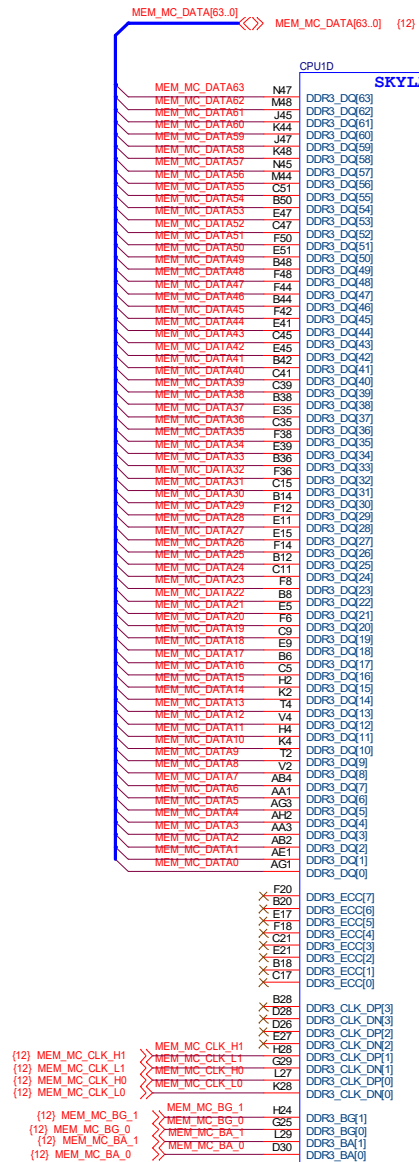


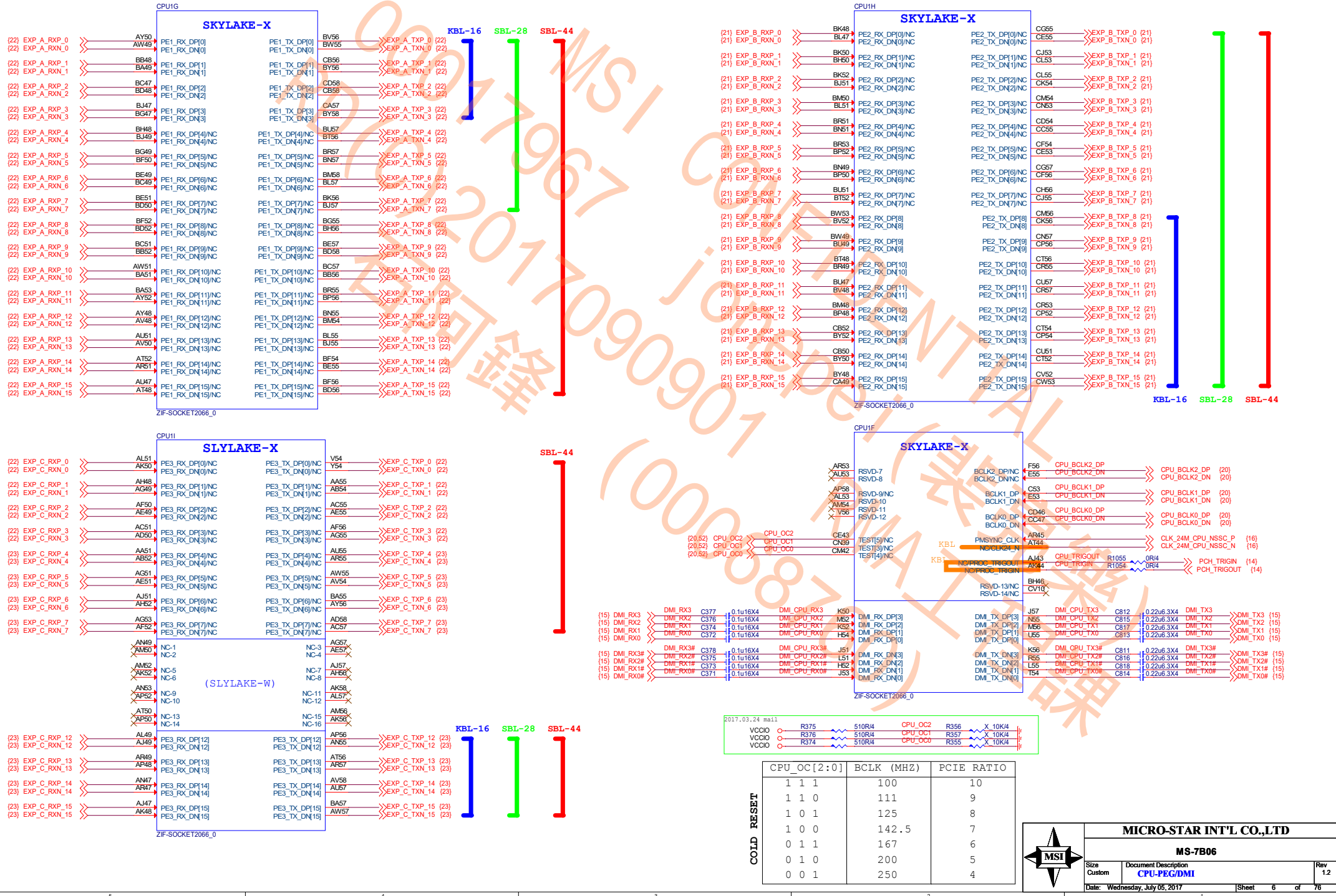


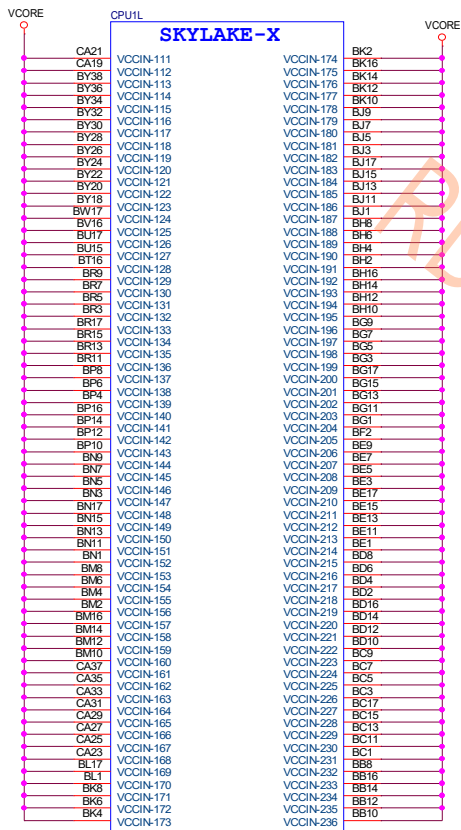
MICRO-STAR INT'L CO.,LTD

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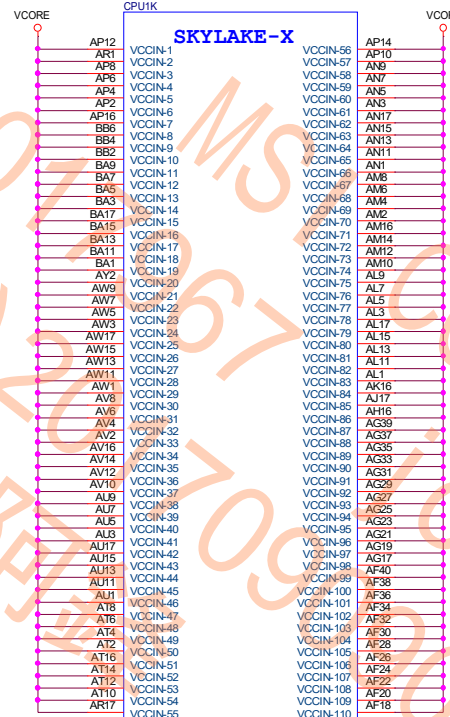
Size	Document Description	Rev
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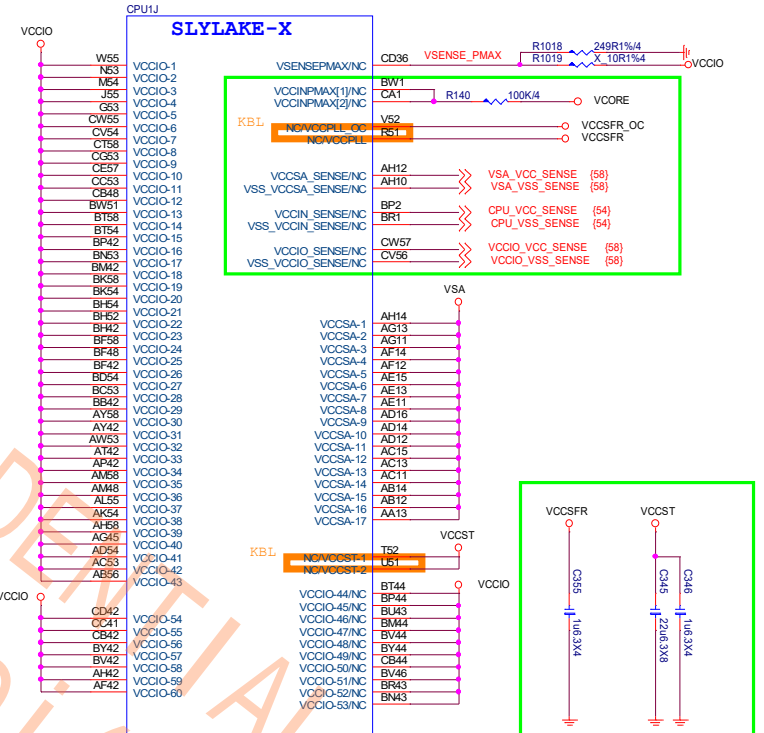




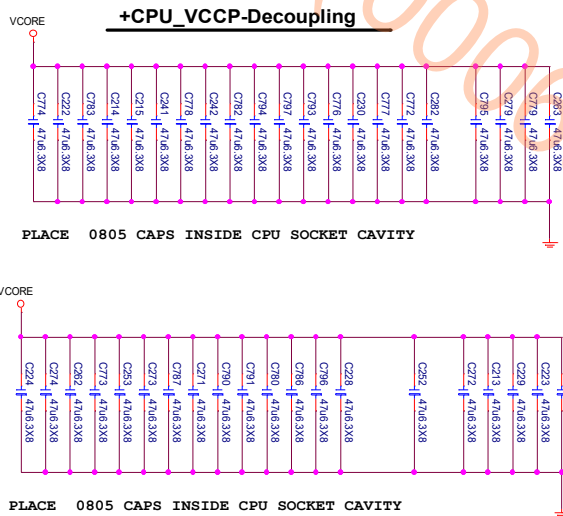
ZIF-SOCKET2066_0



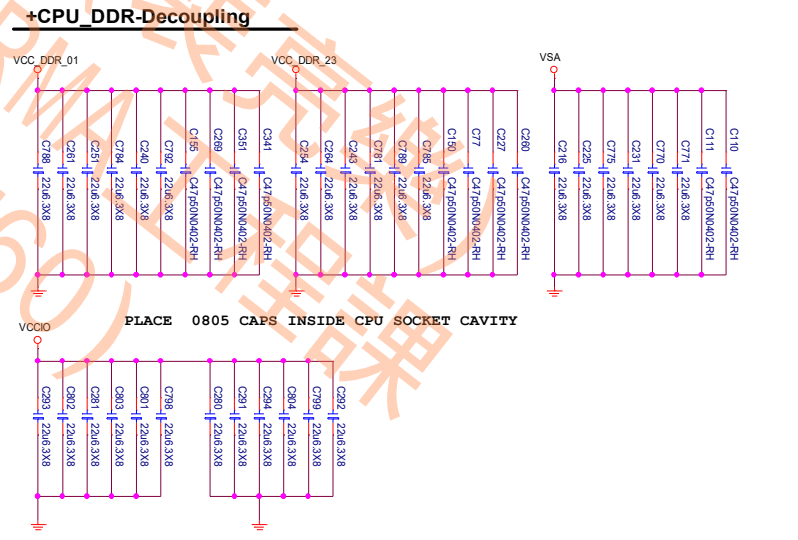
ZIF-SOCKET2066_0



ID For Power Switch ?

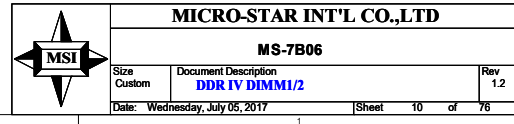


PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

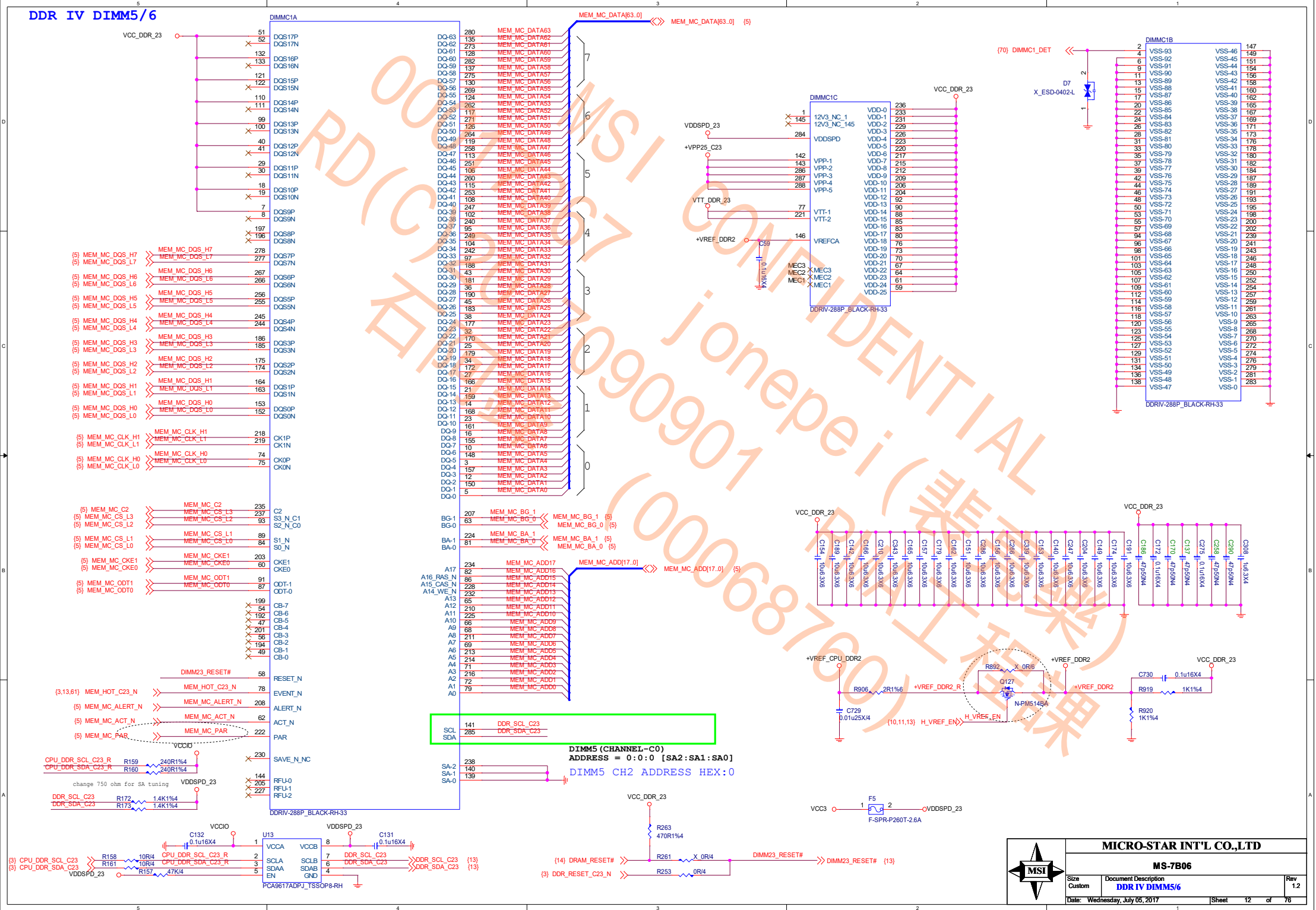


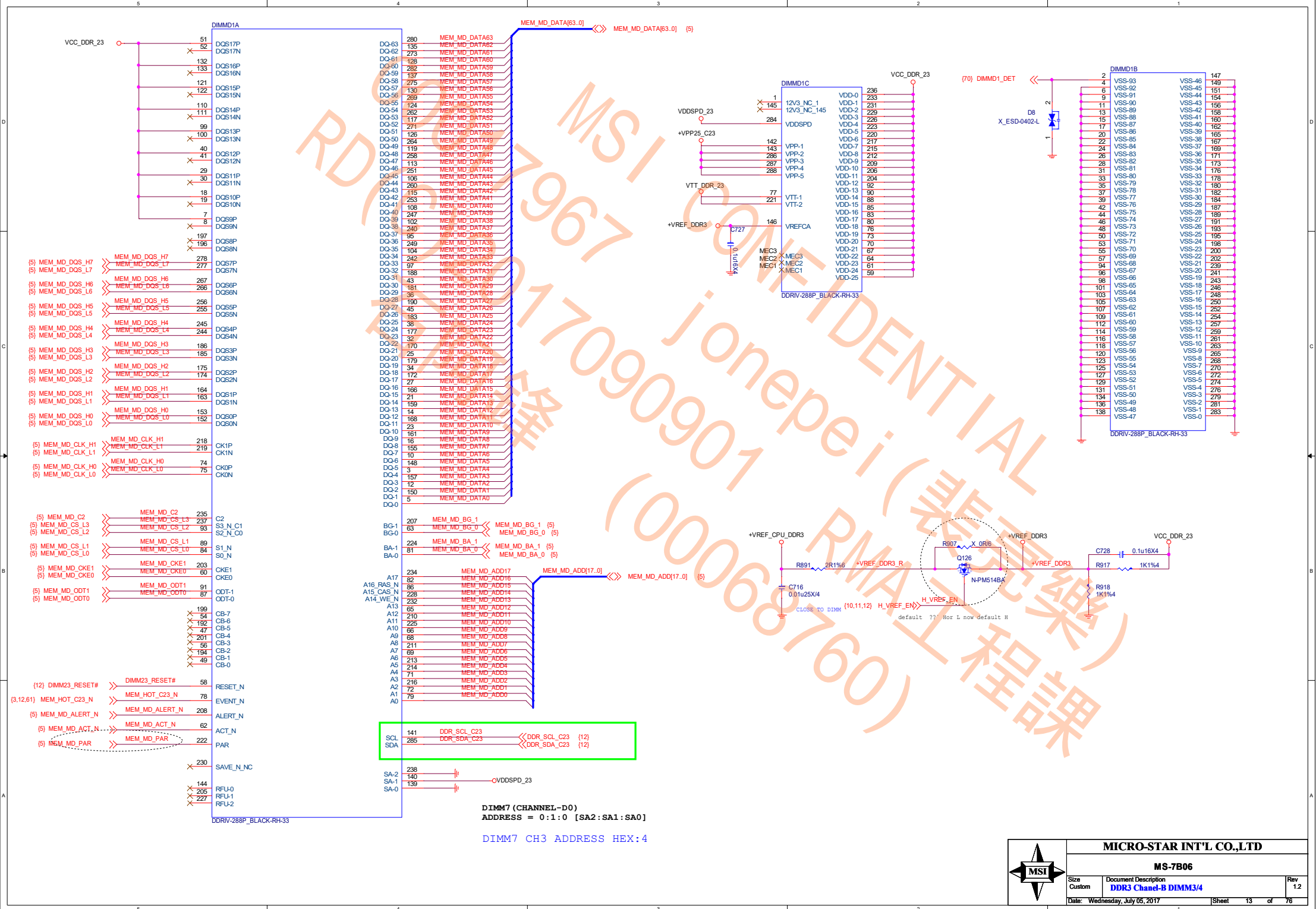
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

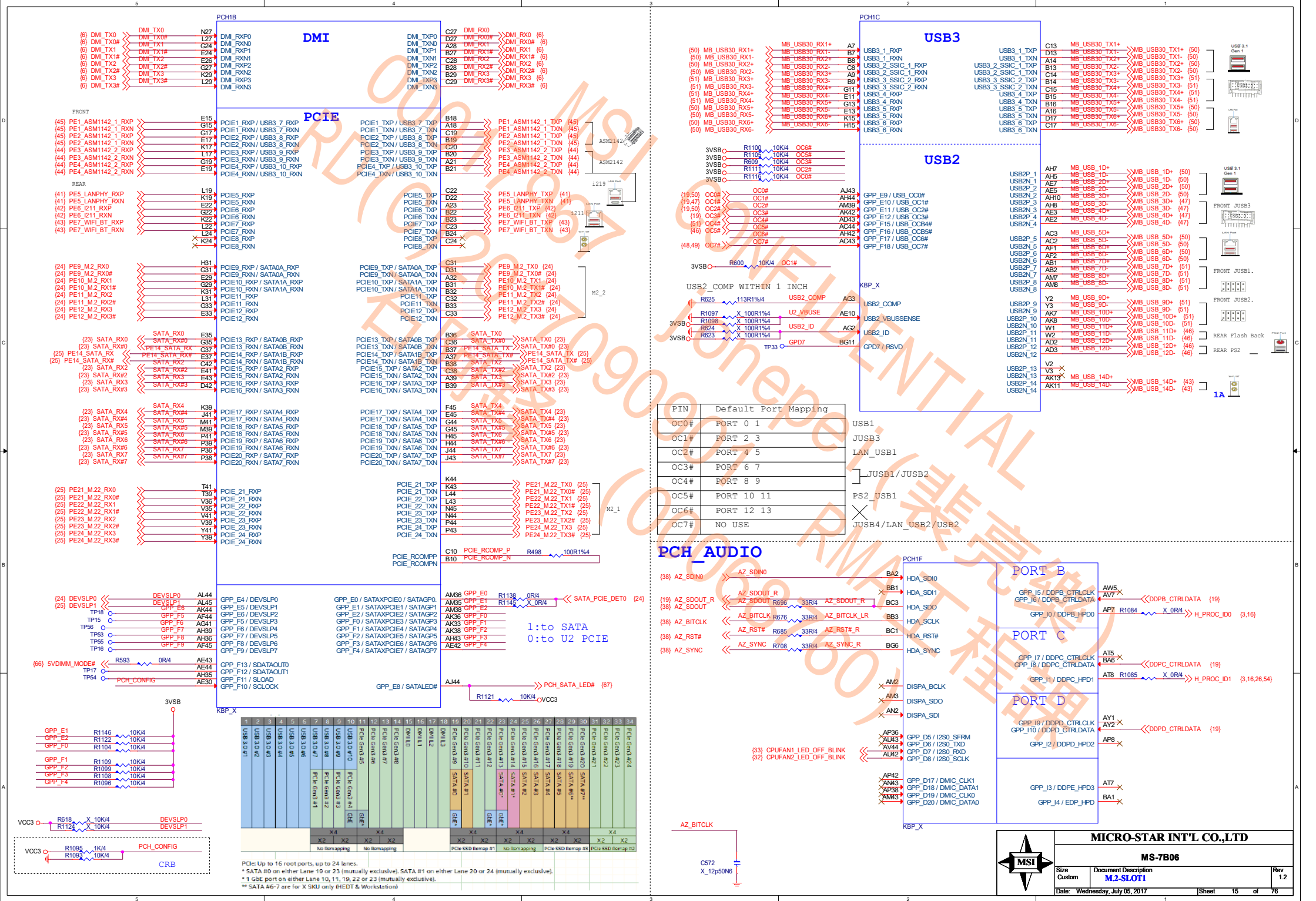
2017.02.13 Ryan mail
DQS9~17P PU to VCC



DDR IV DIMM5/6



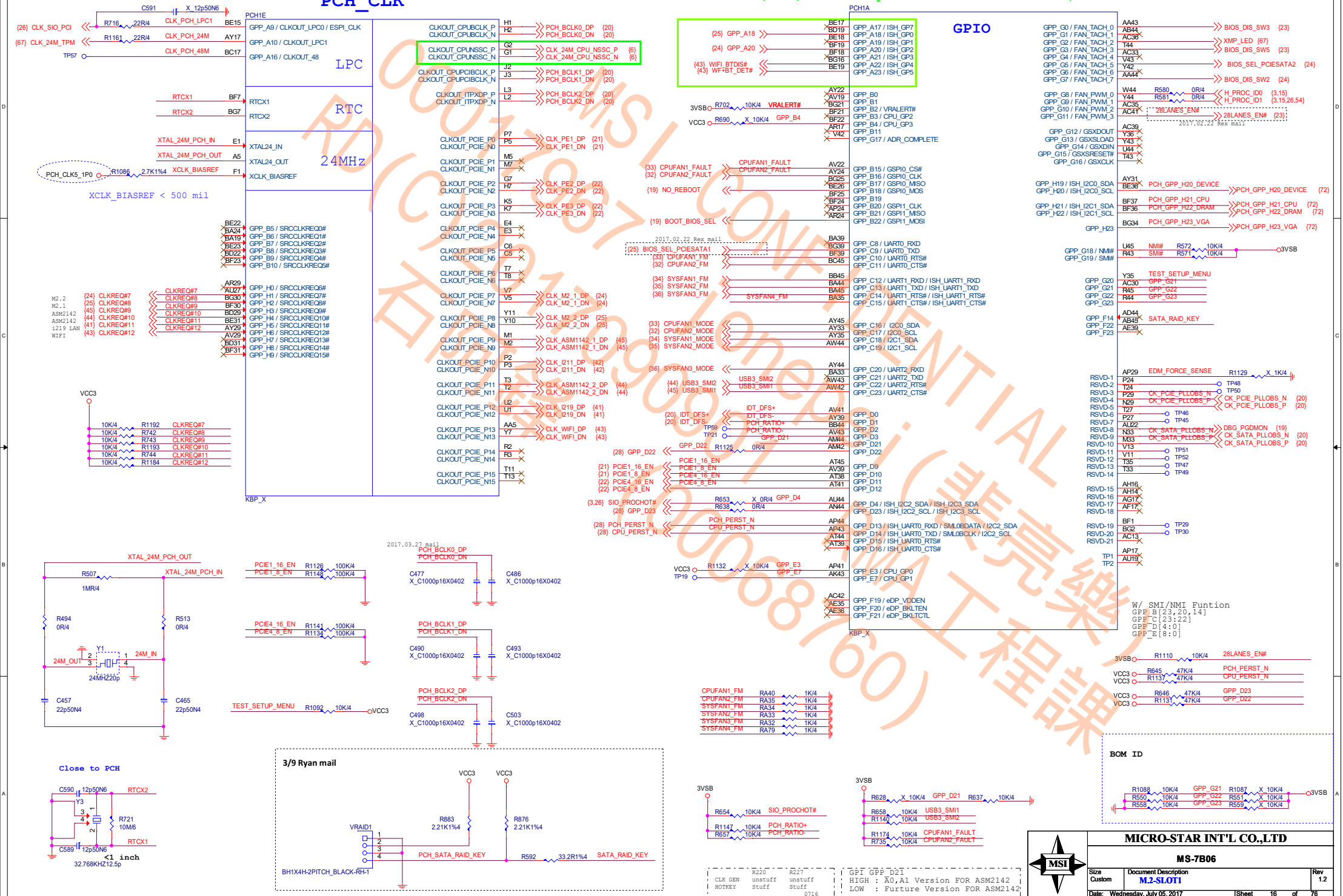


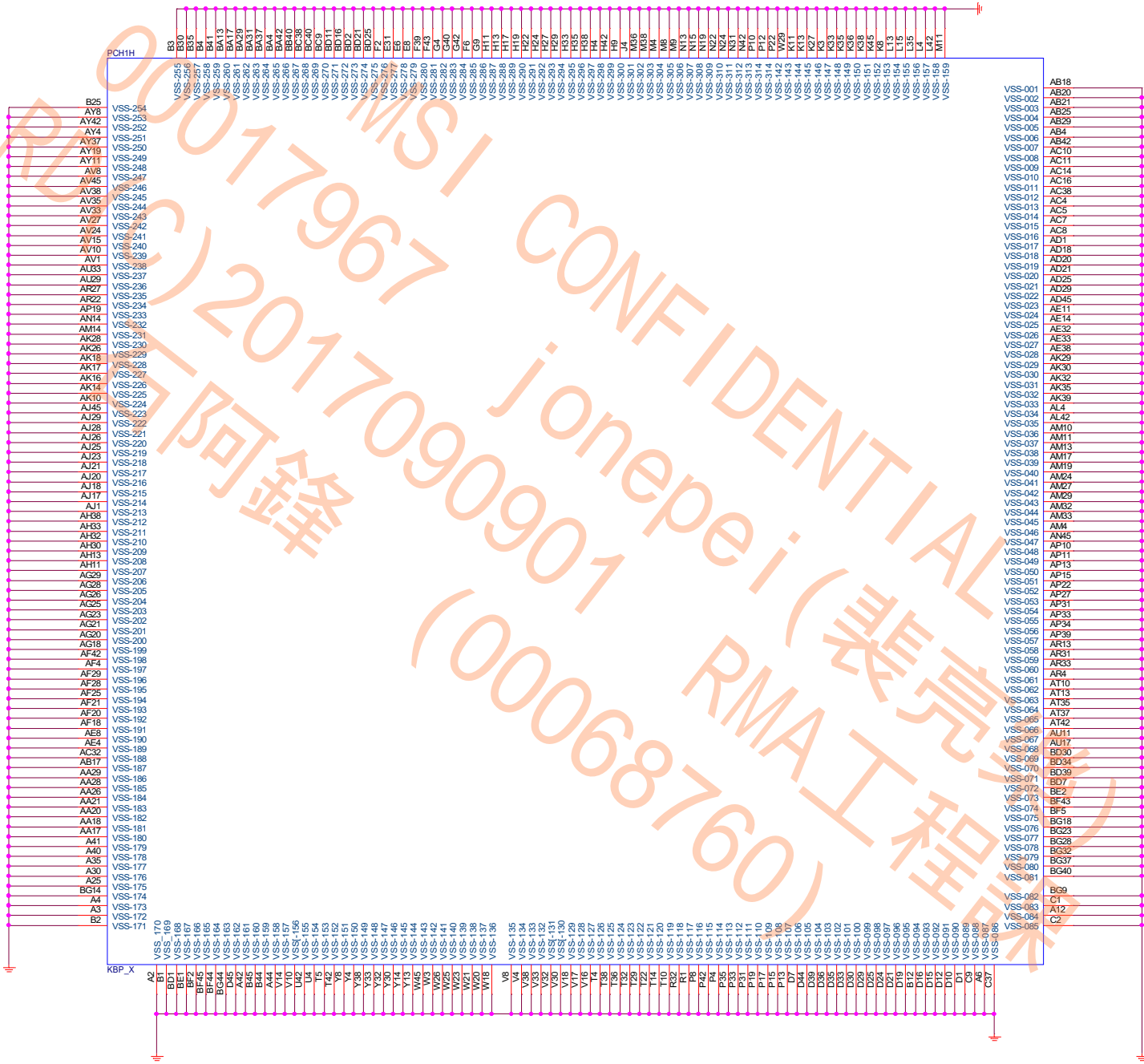


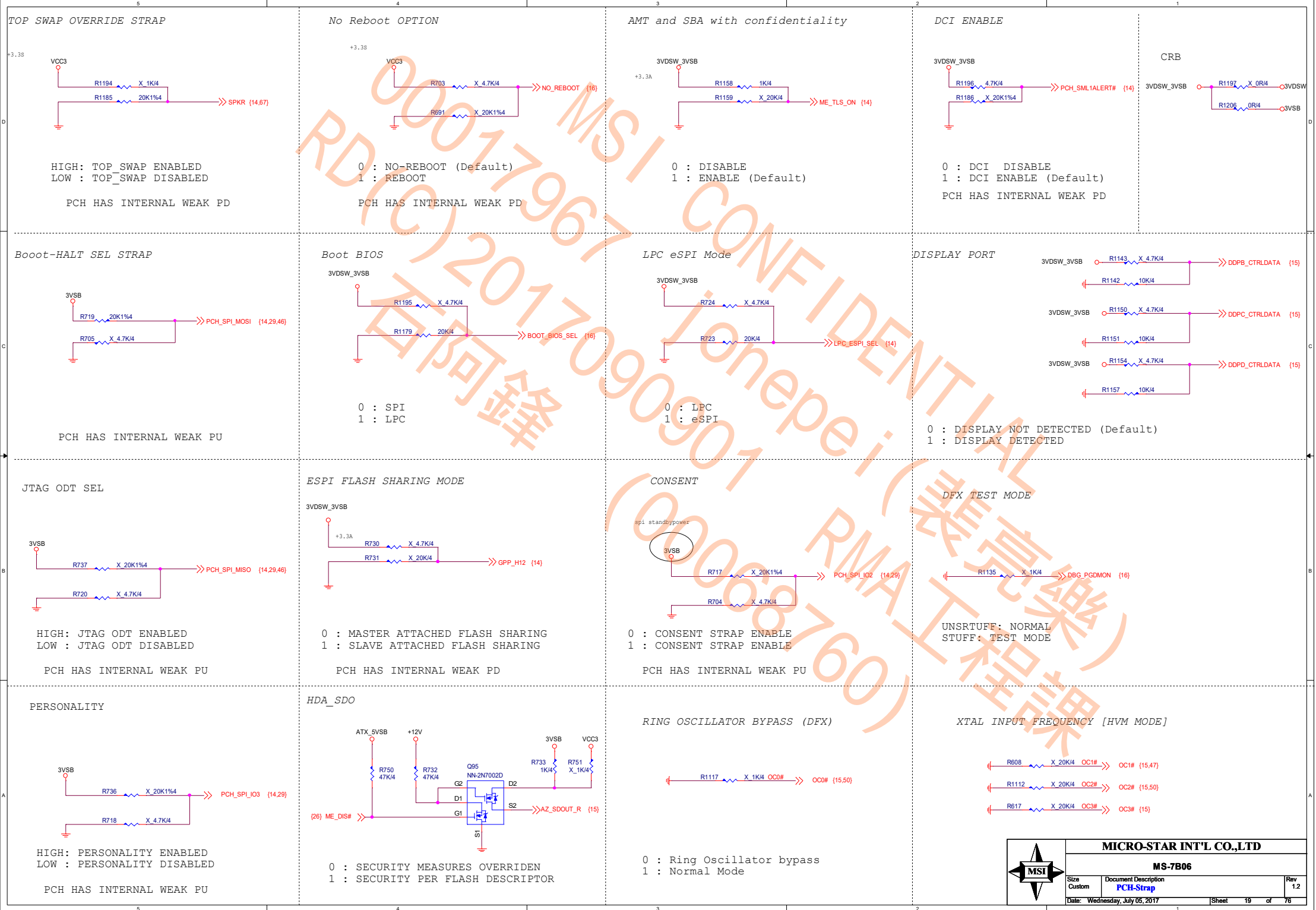
PCH_CLK

Used ESPI(GPPA) GPIO Group A will be come 1.8V leve

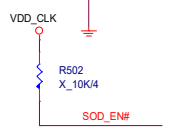
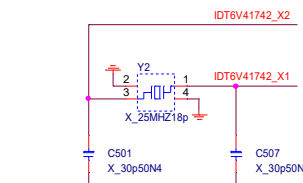
GPIO



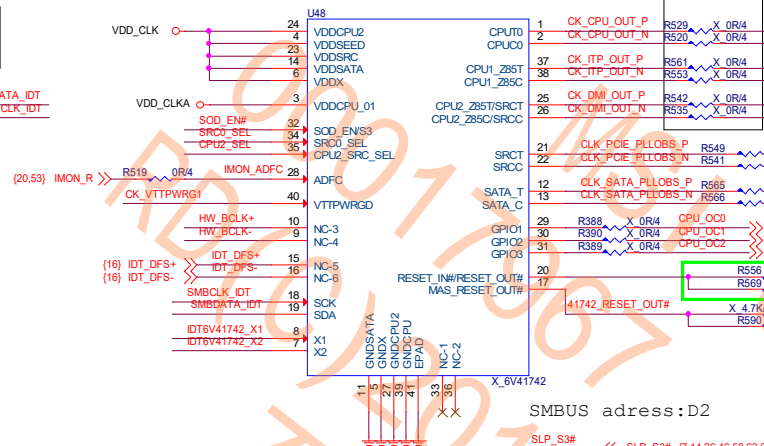




BCLK OC

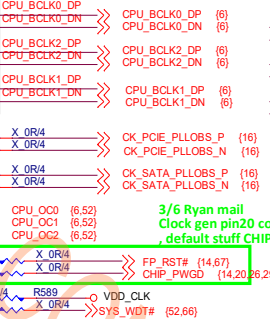


MP此頁全都不上件, 連接PCH CPU CLK的電阻例外

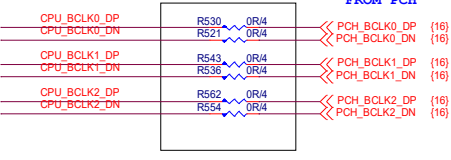


SMBUS address:D2

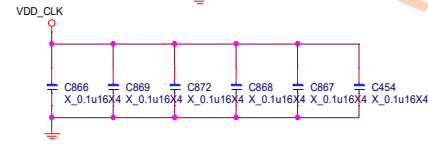
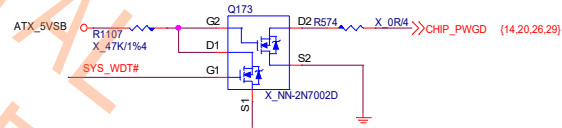
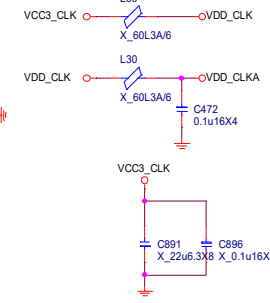
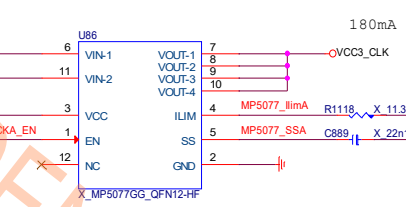
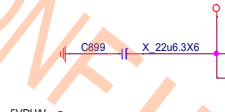
to CPU



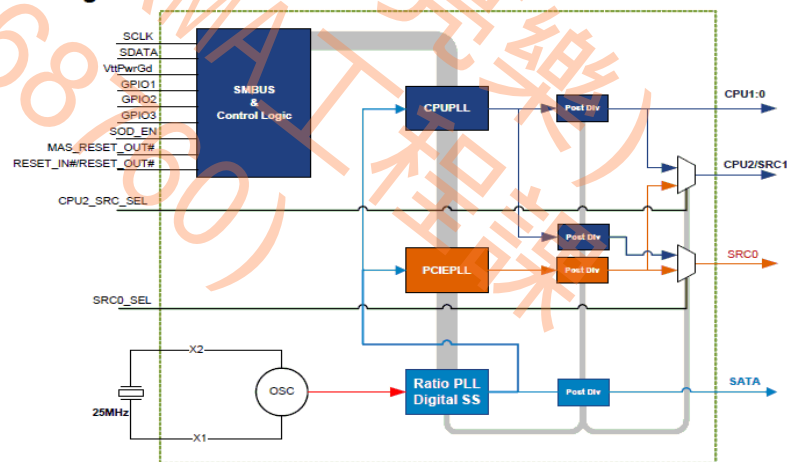
FROM PCH



3/6 Ryan mail
Clock gen pin20 co-lay to CHIP_PWGD
default stuff CHIP_PWGD



Block Diagram

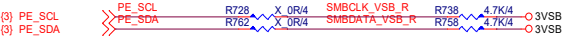
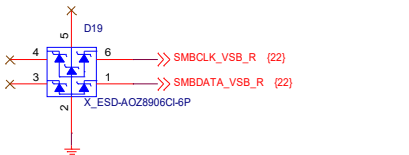


SRC0_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0

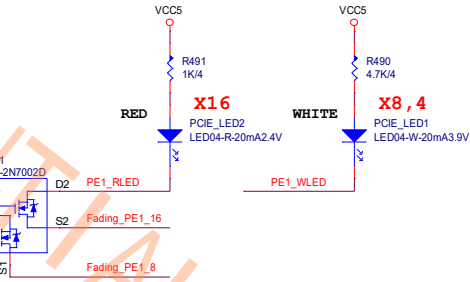
CPU2_SRC_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0

PCIE1 (X16) Slots

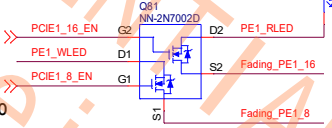
SMBUS ESD



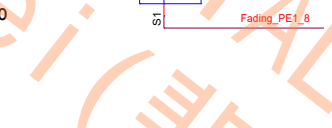
PCIE SLOT LED



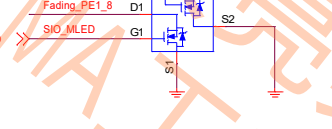
PCH_GPP_D9




PCH_GPP_D10



SIO_PIN98



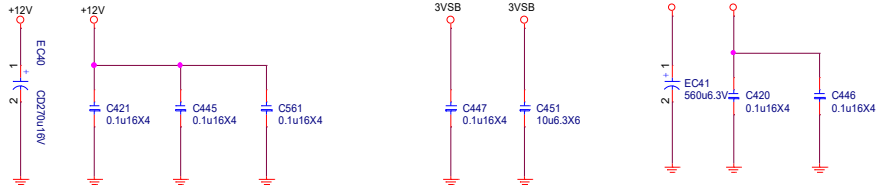
GPIO	GPP_D9	GPP_D10
LED	GPP_D9	GPP_D10
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

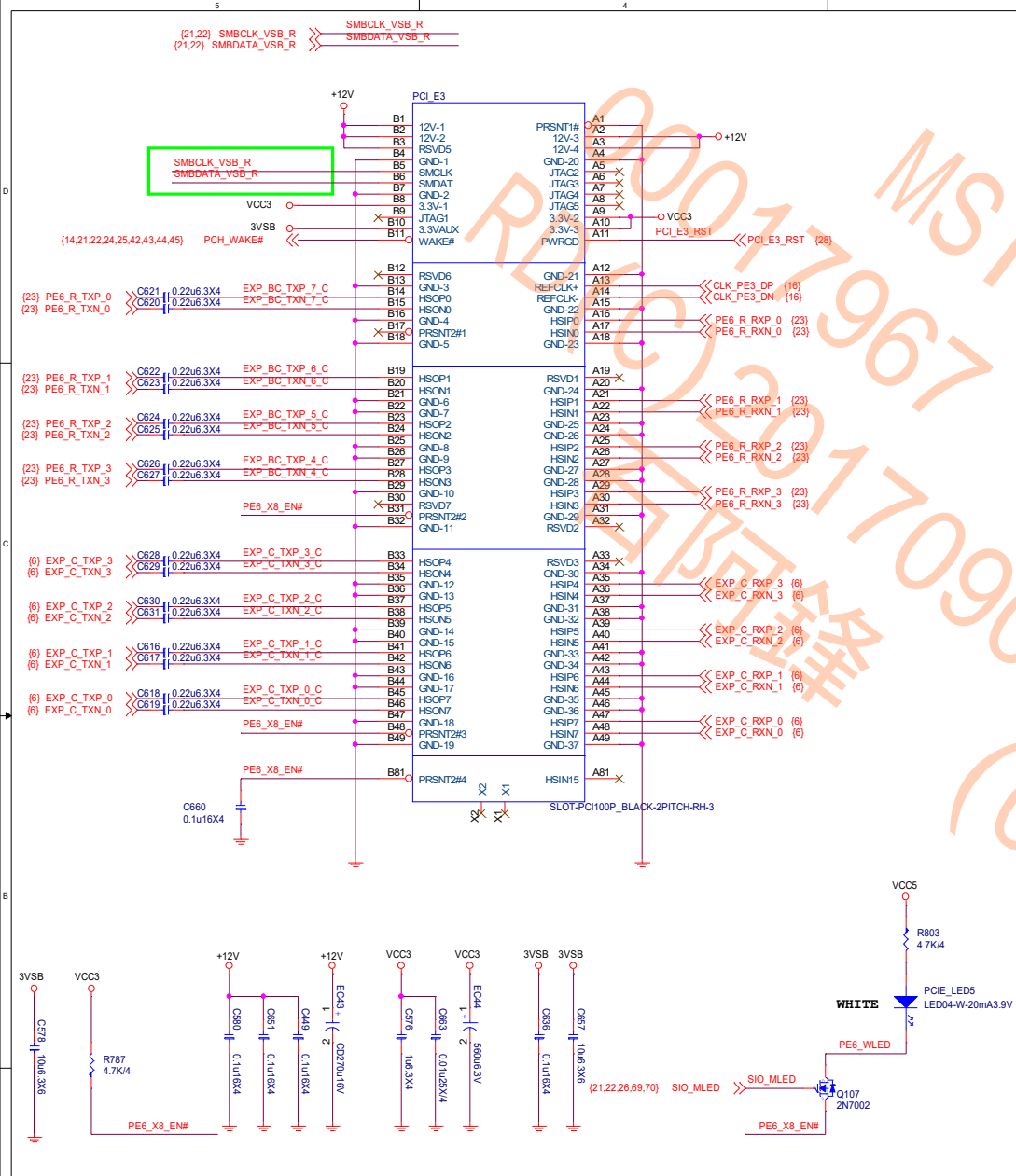


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Custom	PCIE1(X16)Slots	1.2
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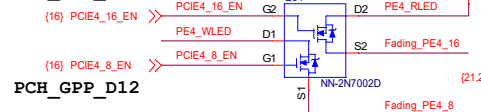




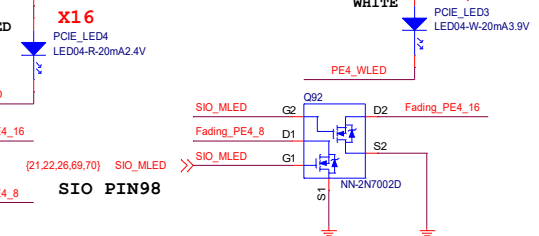
PCIE SLOT LED		
GPIO	GPP_CD11	GPP_D12
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

PCIE OP1
LSI_PCIE_SLOT
X_PCIE_OP1

PCH_GPP_D11



PCH_GPP_D12

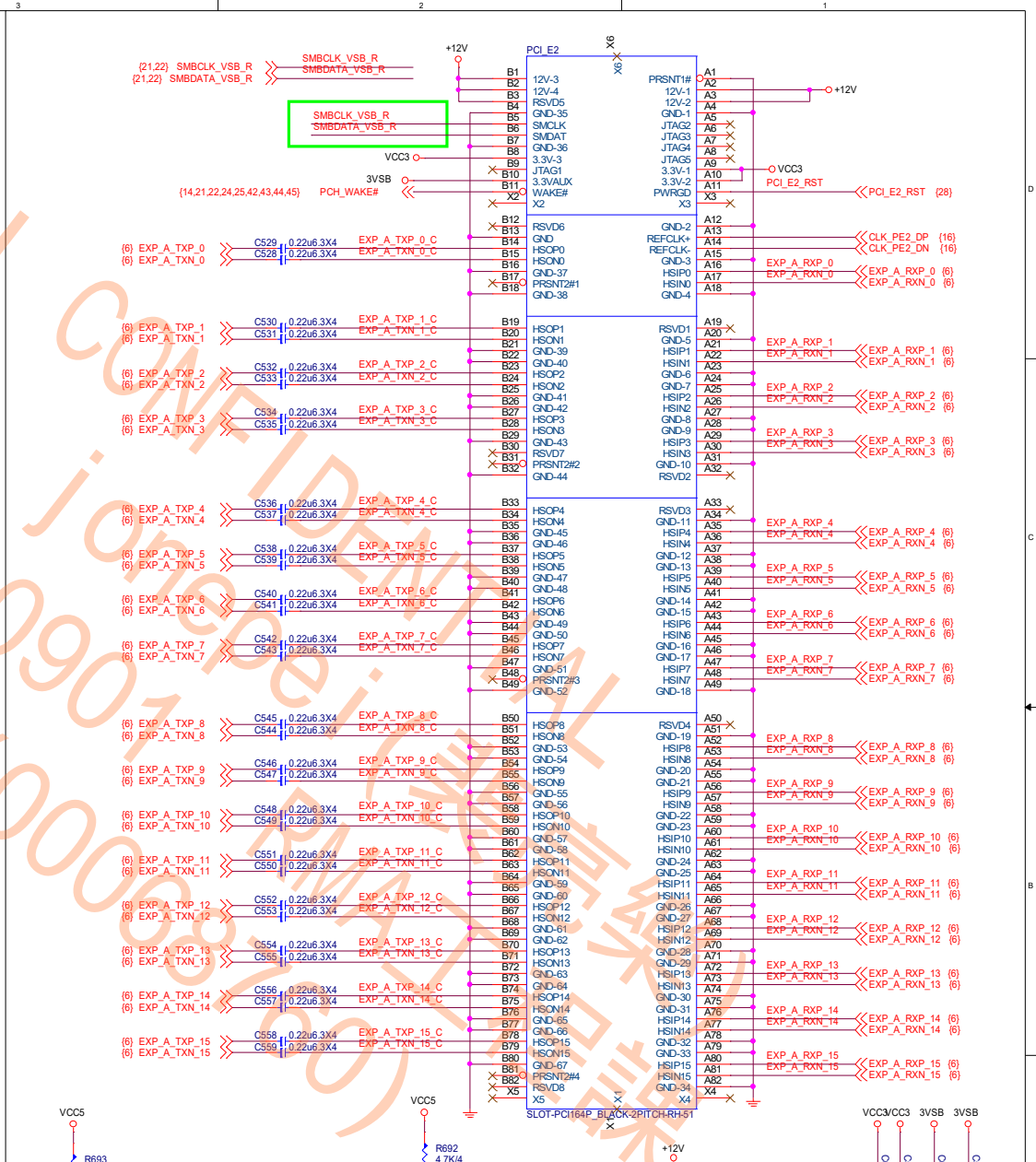


RED
X16
PCIE_LED4
LED04-R-20mA3.9V

WHITE
X8,4
PCIE_LED3
LED04-W-20mA3.9V



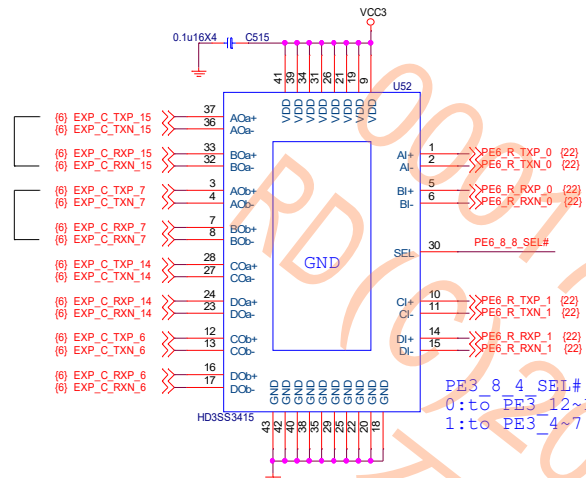
MICRO-STAR INT'L CO.,LTD		
MS-7B06		
Size Custom	Document Description PCIE2(X16)	Rev 1.2
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SEL:
0:28
1:44

From:PE3_12~15

From:PE3_4~7



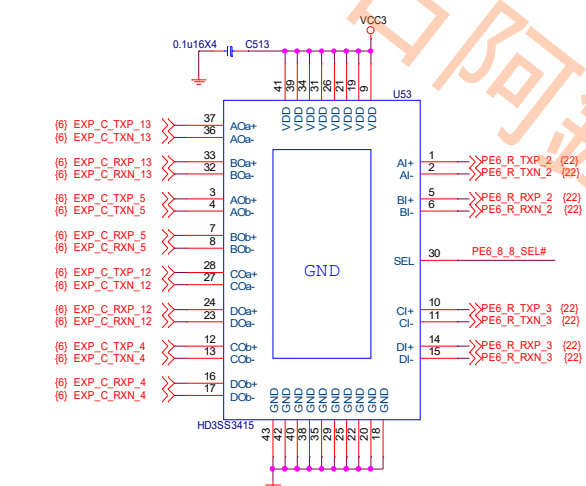
PE3 8 4 SEL#:
0:to PE3_12~15(28lanes by 4)
1:to PE3_4~7(44lanes by 8)

BIOS_DIS_SW3	BIOS_DIS_SW5	PE6_8_SEL#
0	1	0
0	0	1

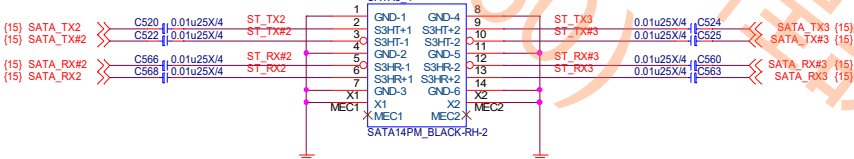
28
44

H_PROC_ID1	28LANES_EN#	PE6_8_SEL#
1	1	1
1	0	0

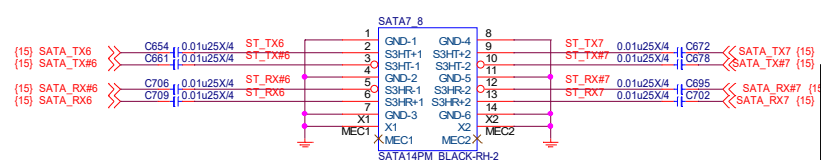
44Lanes
28Lanes



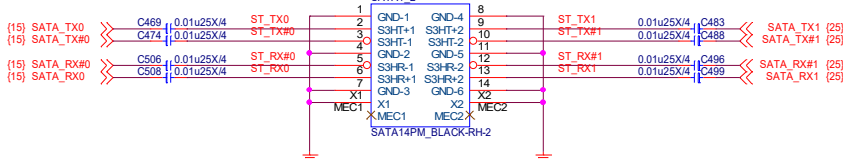
SATA 6G PORT 2.3



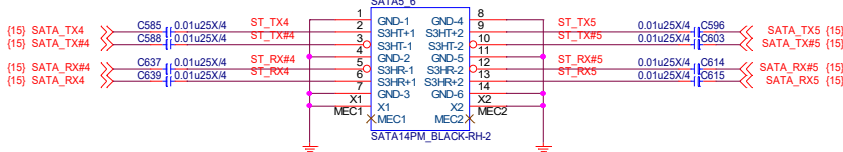
SATA 6G PORT 6.7




SATA 6G PORT 0.1



SATA 6G PORT 4.5

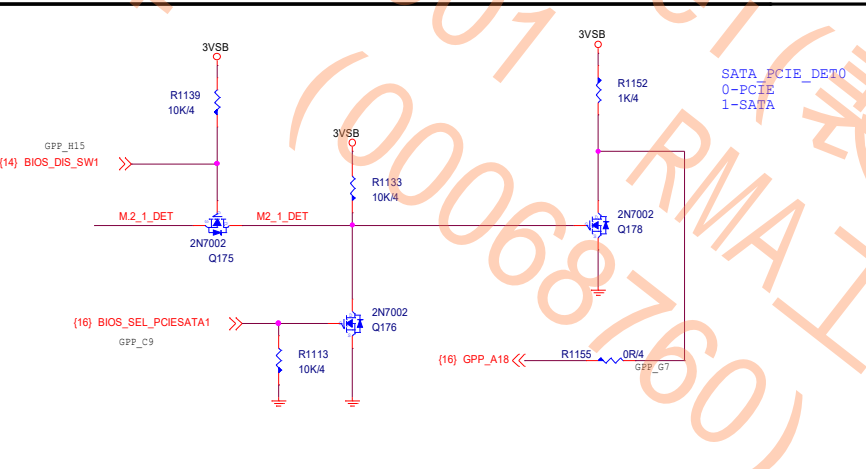
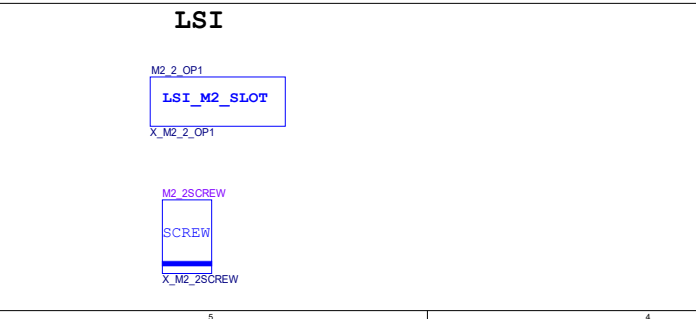
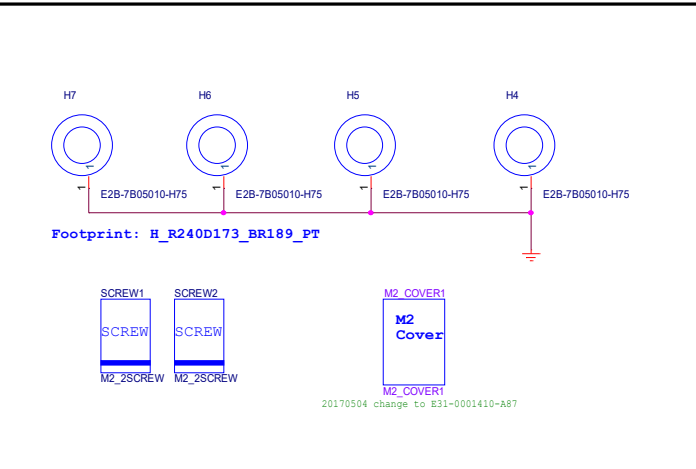
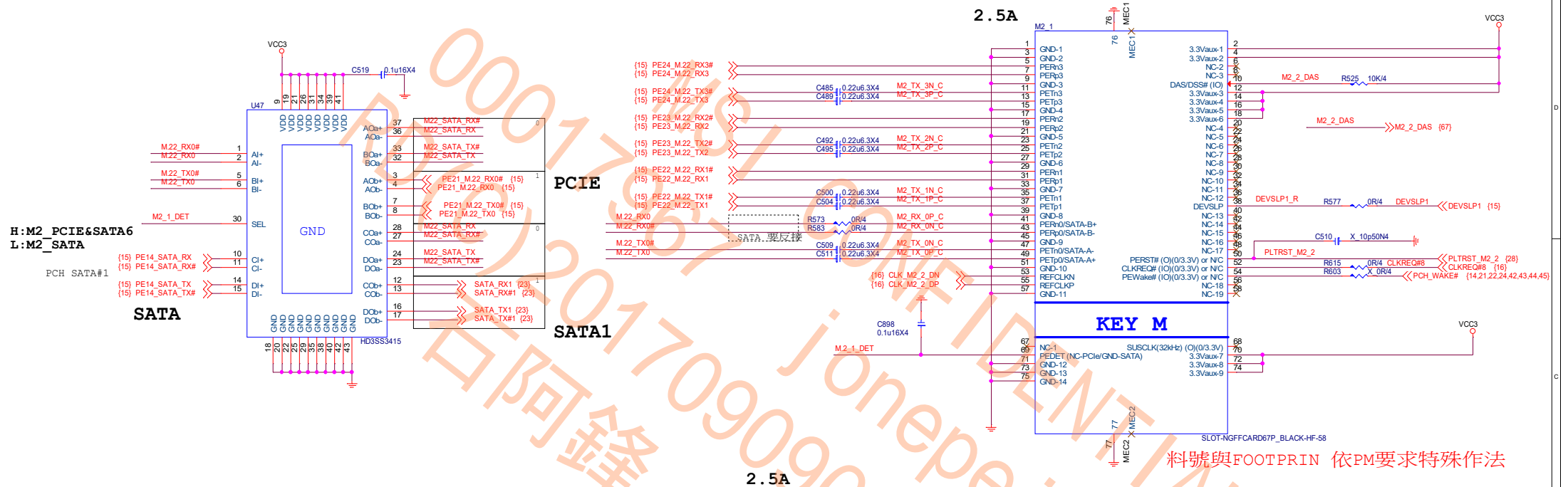




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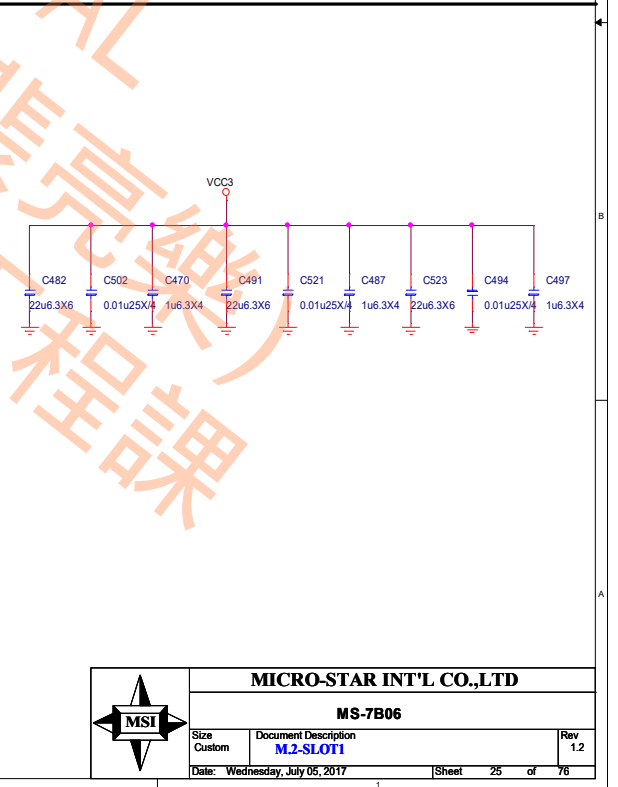
MS-7B06

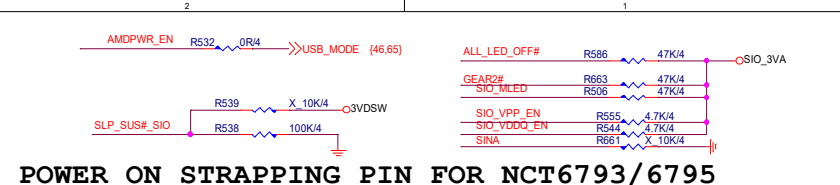
Size Custom	Document Description PCI-E-SWITCH	Rev 1.2
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BIOS_MODE

GPP_H15 BIOS_DIS_SW1	GPP_C9 BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI (1)	0	AUTO





PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

SIO_VCC3

R534 X 1K/4 R557 680R/4
 R545 X 1K/4 DTRB# R560 680R/4
 R659 1K/4 RTSAB# R642 X 680R/4
 R670 1K/4 SOUTA R62Z X 680R/4

SIO_3VA

R640 1K/4 DSW_EN R539 X 680R/4
 R523 X 1K/4 AMPDPWR_EN R659 680R/4
 TESTMODE R631 680R/4
 R570 680R/4

SIO_VCC3

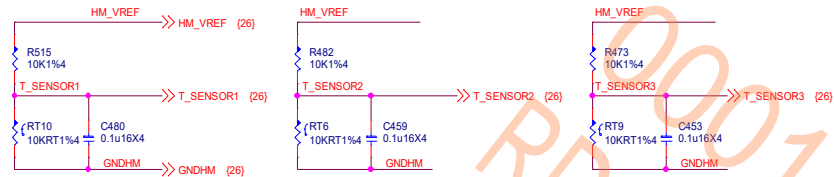
R660 X 1K/4 DTRA# R651 680R/4

Intel
 6793 pull down
 6795 pull down

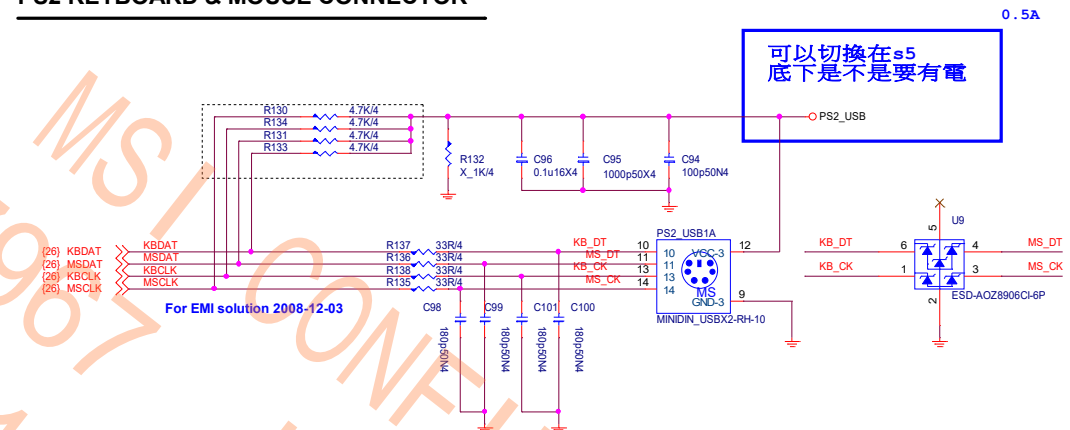
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MS-7B06			
Size Custom	Document Description SIO-NCT6793D-1		Rev 1.2
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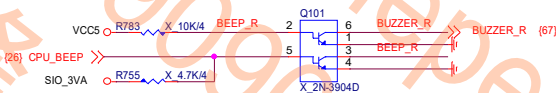
THERMAL



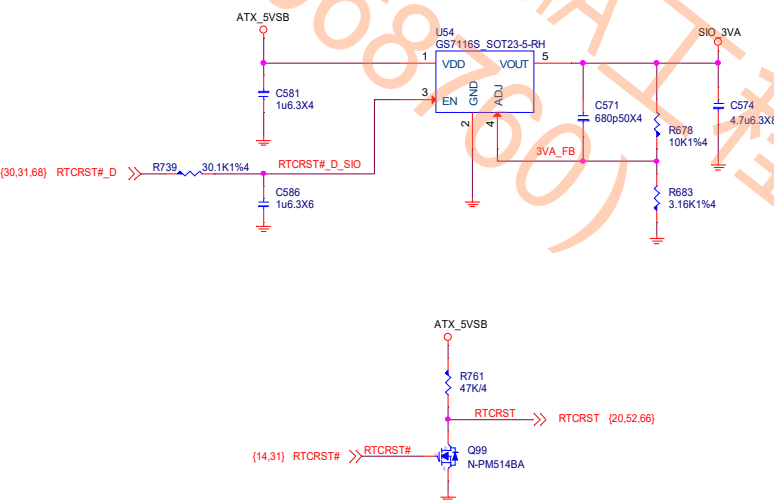
PS2 KEYBOARD & MOUSE CONNECTOR



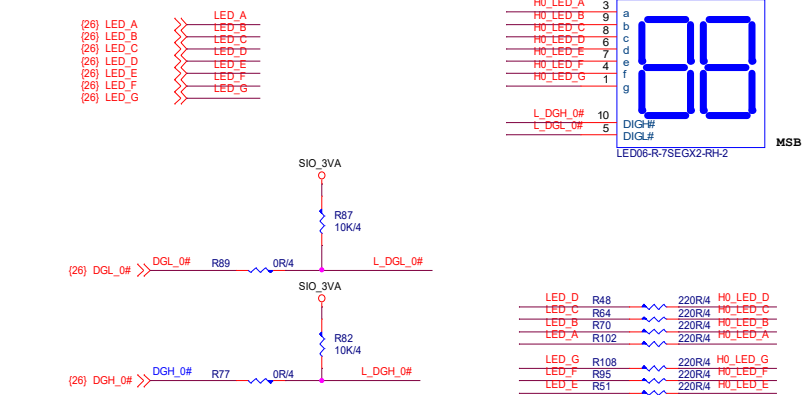
COM Port for BIOS Debug



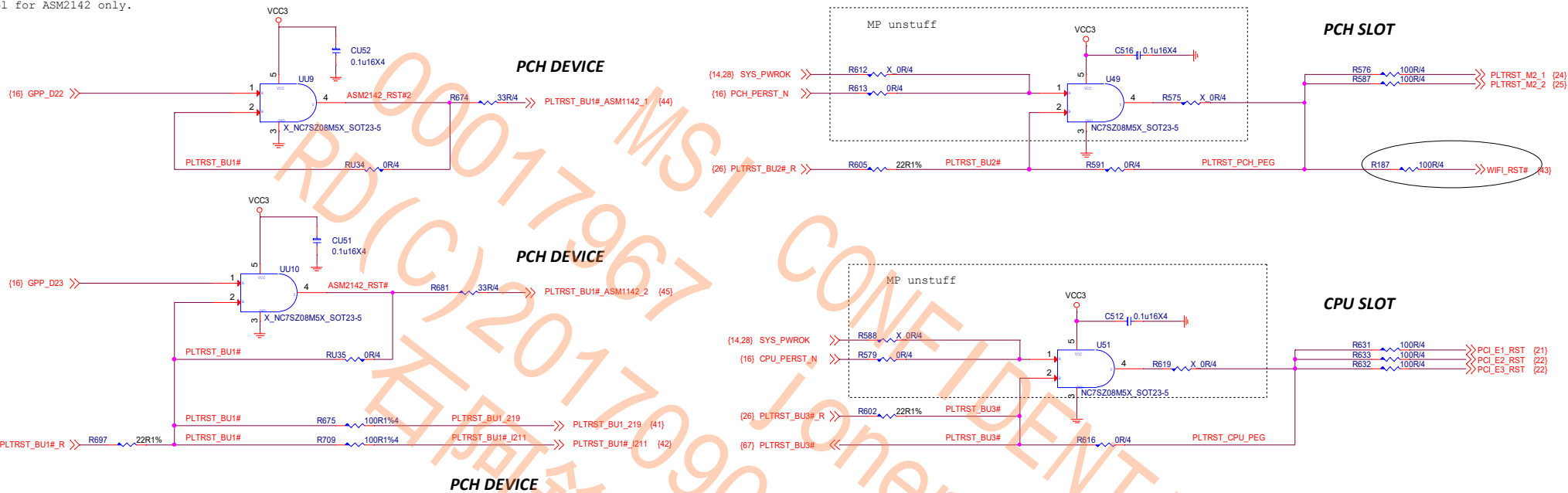
SLP_SUS Co-lay circuit



DEBUG LED

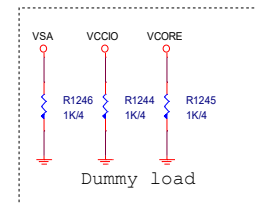
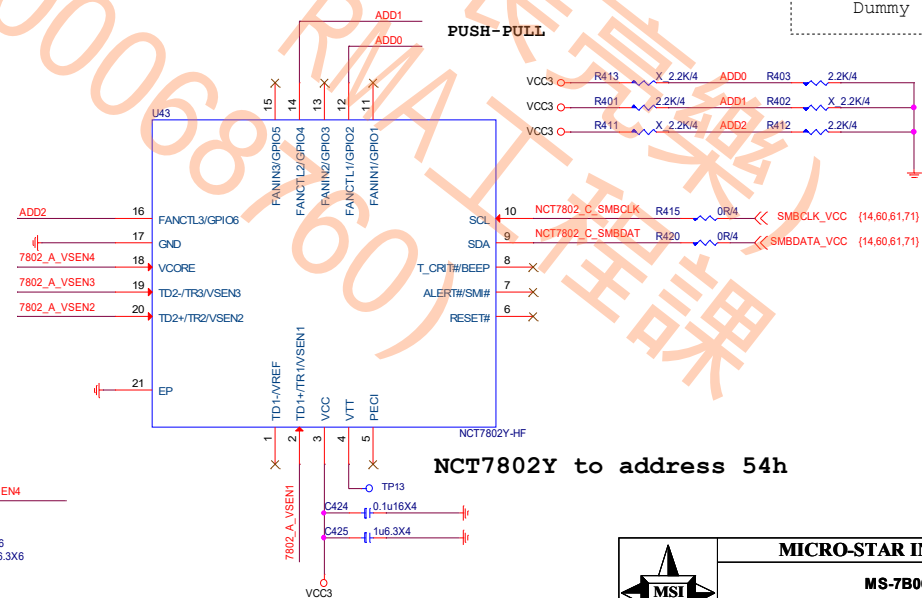
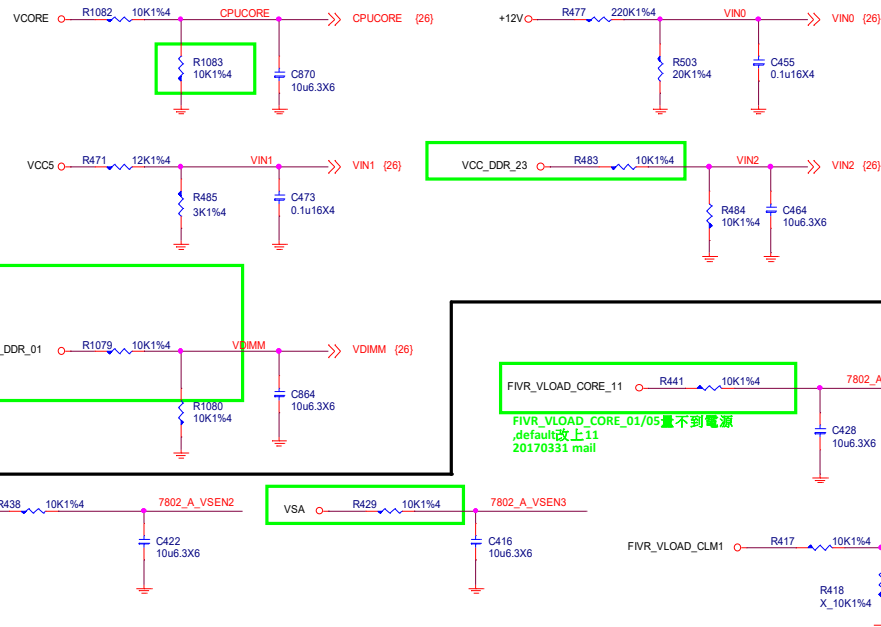


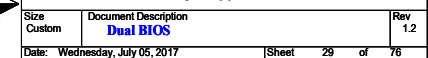
Reset control for ASM2142 only.



HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect





Skylake/Kabylake Path Circuit For Dual Bios

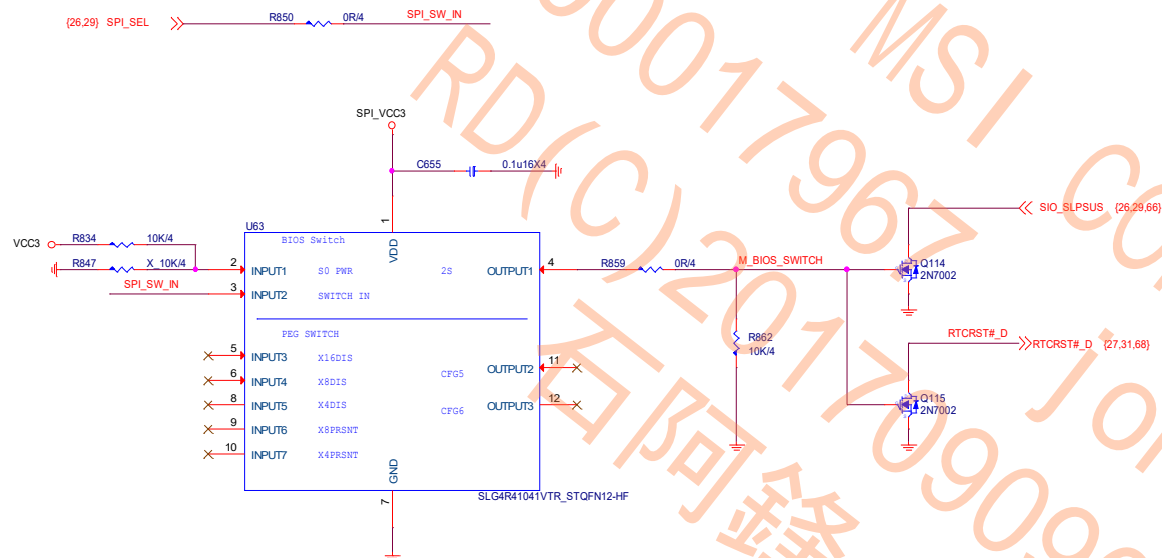


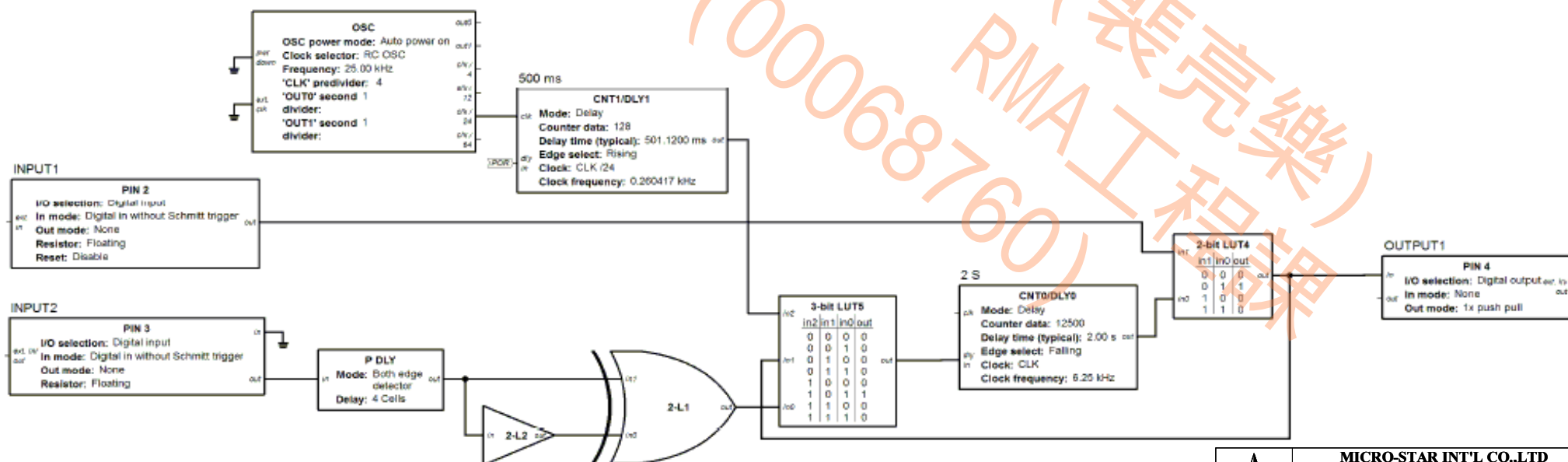
TABLE 1. Function 1

Function1		
INPUT1(PIN2)	INPUT2(PIN3)	OUTPUT1(PIN4)
X	Hi → Low	Hi (keep 2S)
X	Low → Hi	Hi (keep 2S)
Hi	X	Low

TABLE 2. Function 2

Function2						
INPUT3(PIN5)	INPUT4(PIN8)	INPUT5(PIN8)	INPUT6(PIN9)	INPUT7(PIN10)	OUTPUT2(PIN11)	OUTPUT3(PIN12)
1	1	1	1	1	0	0
1	1	1	0	1	1	0
1	1	1	X	0	1	1
1	1	0	X	X	1	0
1	0	X	X	X	0	0
0	X	X	X	X	0	0

Block Diagram



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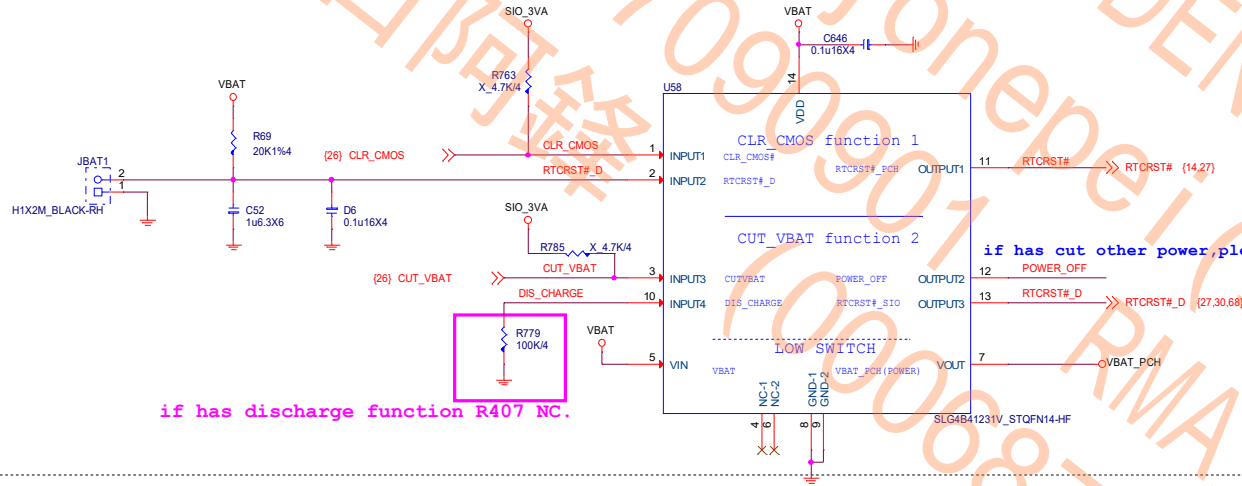
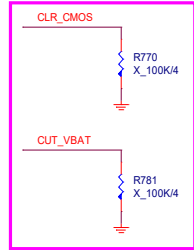
MS-7B06

Size Custom	Document Description Dual bios control-Silego	Rev 1.2
Date: Wednesday, July 05, 2017		Sheet 30 of 76

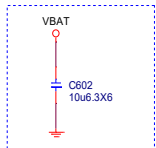
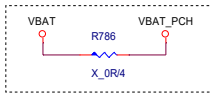
RTCST# R778 X_OR/4 RTCST#_D

CUT_VBAT

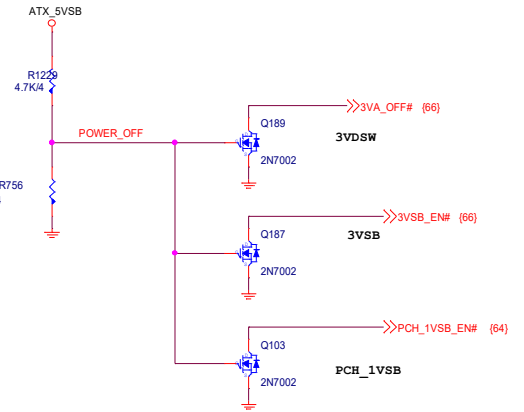
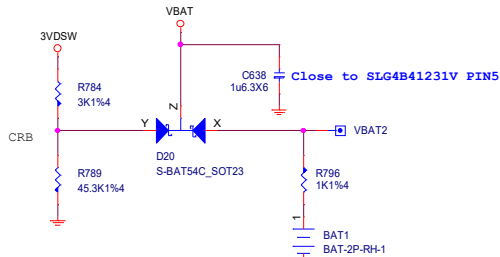
20160629



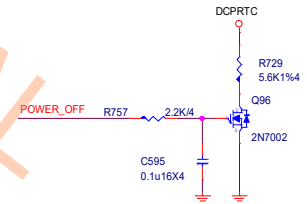
VBAT



have timing issue keep 0805 size don't removed



Add DCRTC discharge circuit



TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

From SIO
(26) SIO_CPU_FAN1

(16) CPUFAN1_MODE

FIX MODE unstuff

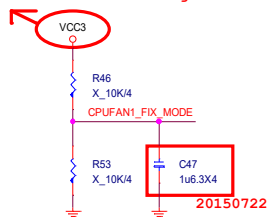
PWM Mode : VOUT voltage follows VIN voltage
DC Mode : VOUT voltage is regulated to 3.8*DCIN voltage.

GPIO Control

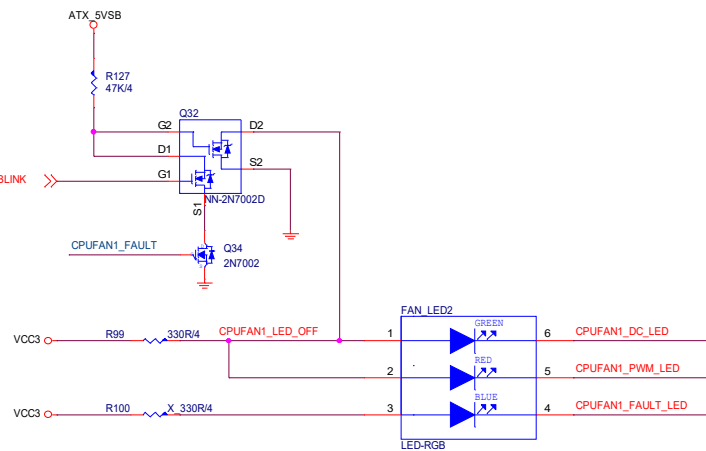
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)
Internal pull up 1.65V	

Default

Avoid NCT3947S MODE PIN Leakage



Resever For FIX DC or PWM MODE USE By PM SPEC



RGB
D0C-040S400-H91
DC_FAN_LED (綠)
PWM_FAN_LED (藍)
FAN_OCP_LED (紅)

Forward Current 20mA
Pulse Forward Current 40-60mA

C_FAN1_PWM R59 100R/4

C50 X 0.1u16X4

+12V >80mil

C48 0.1u16X4

D5 1N4148W

R67 4.7K/4

R57 27K/4

C49 X_0.1u16X4

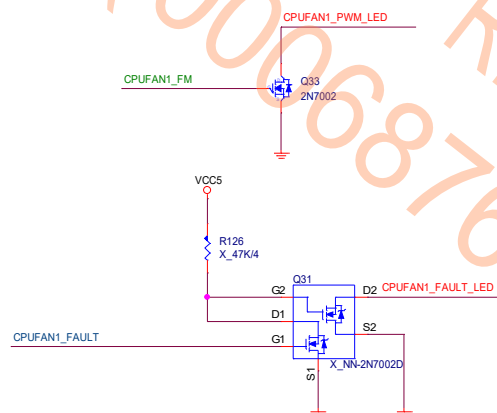
R58 10K/4

TO SIO
CPU1_FAN1 (26)

CPUFAN_PWR
>40mil

C22,C23,C263 close to FAN Connector

CHECK NCT3947S Sink Current



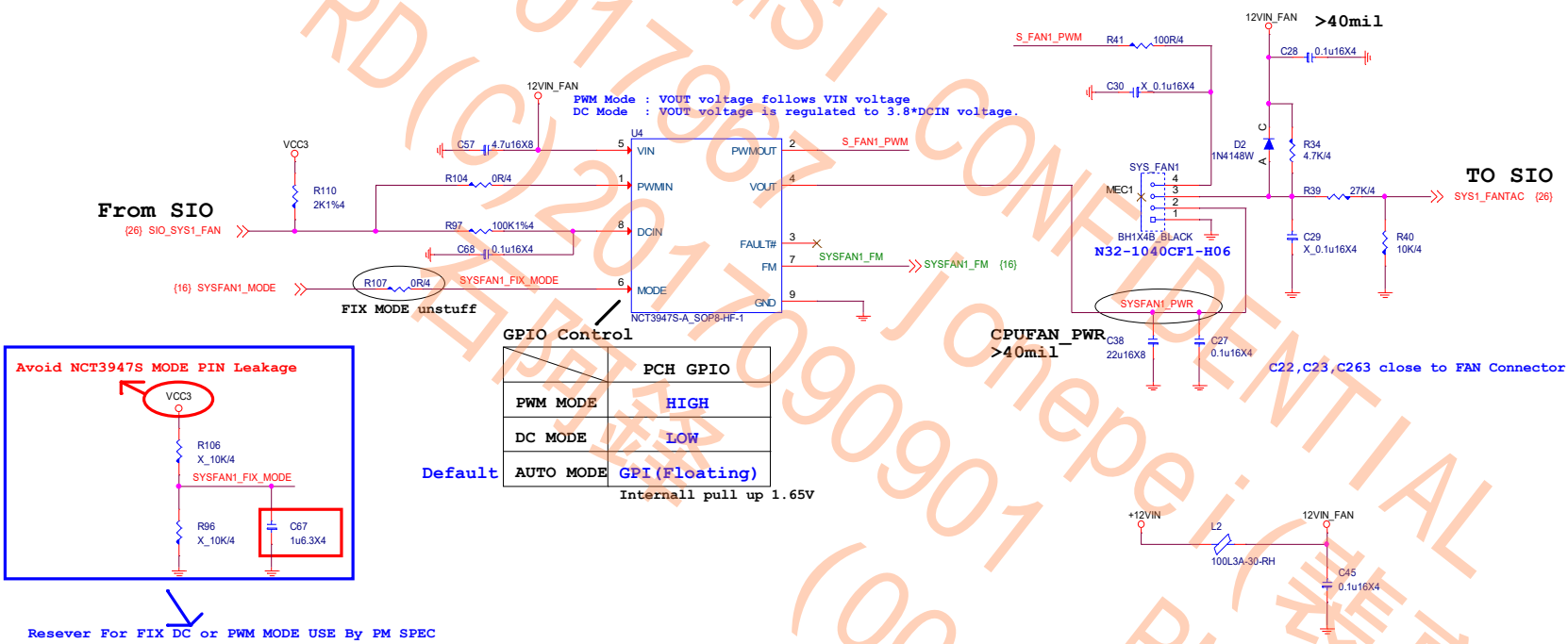
MICRO-STAR INT'L CO.,LTD

MS-7B06

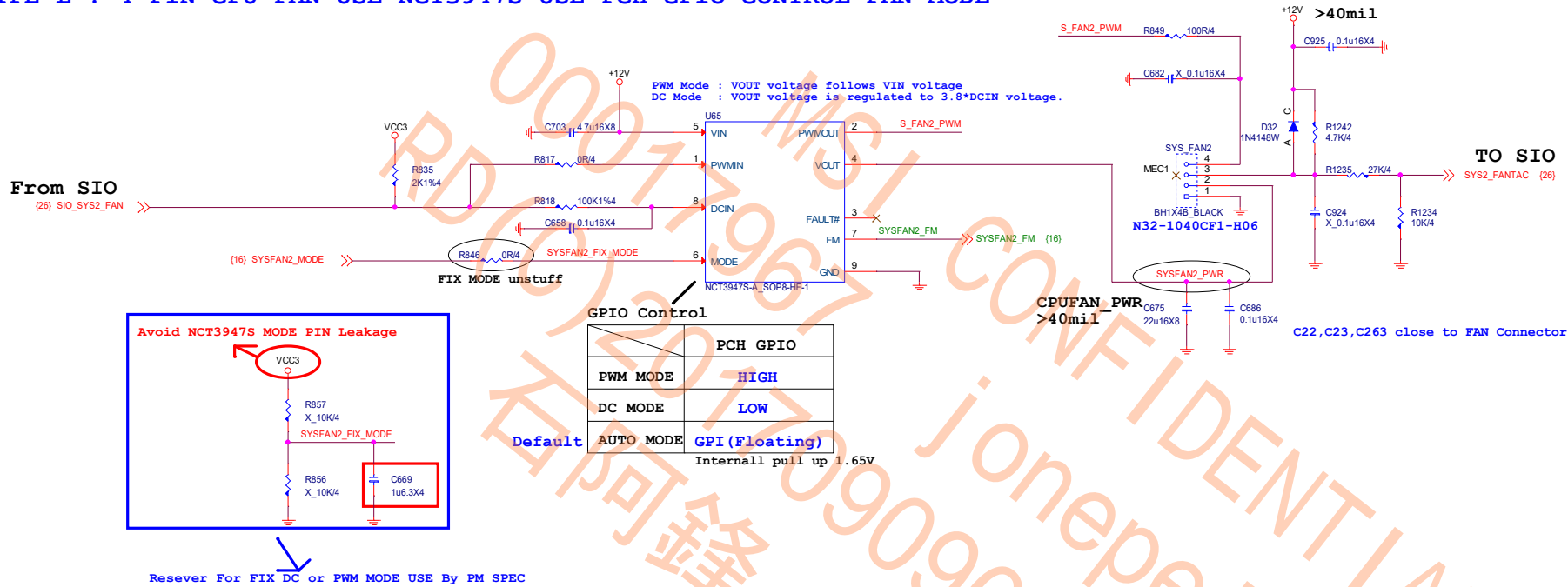
Size	Custom	Document Description	Rev
		CPU FAN1	1.2
Date:	Wednesday, July 05, 2017	Sheet	33 of 76

TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

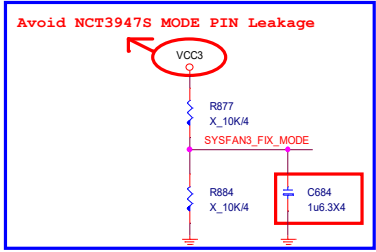
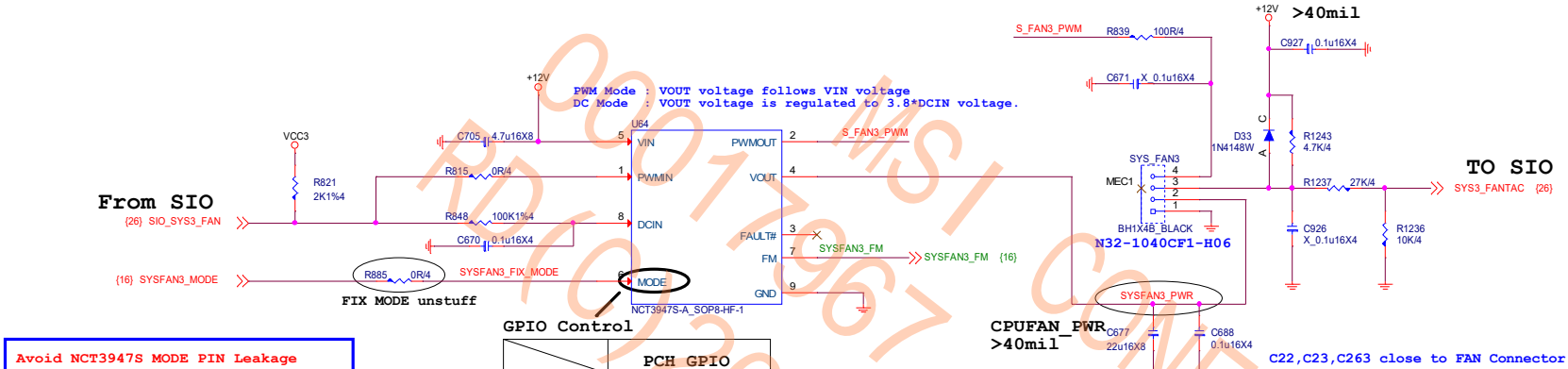
- 1.Mode GPIO BIOS can swtich PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE



TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

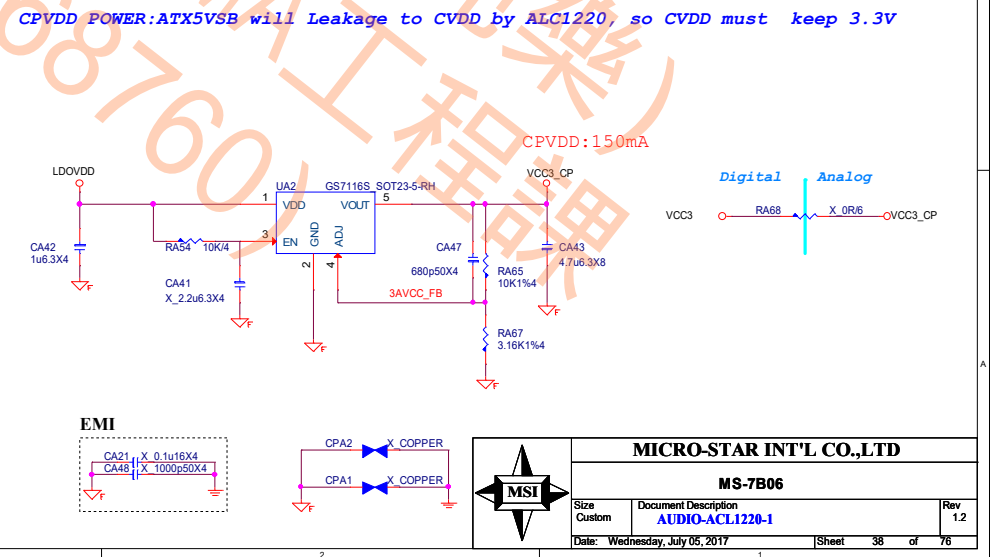
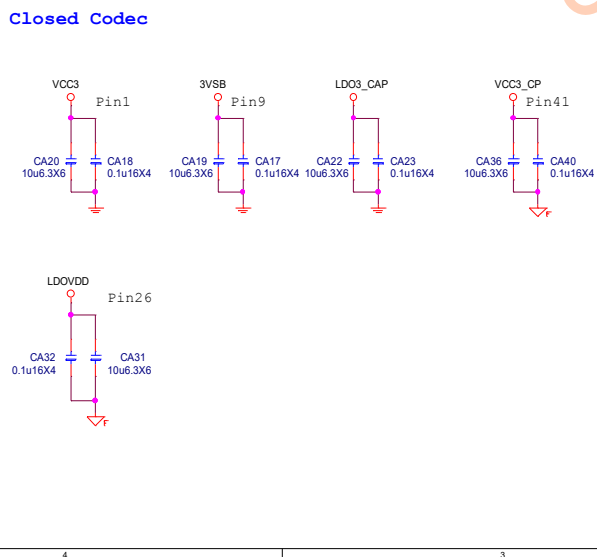
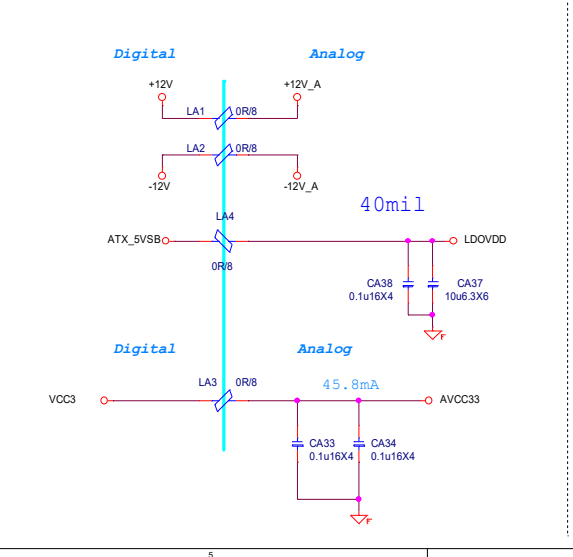
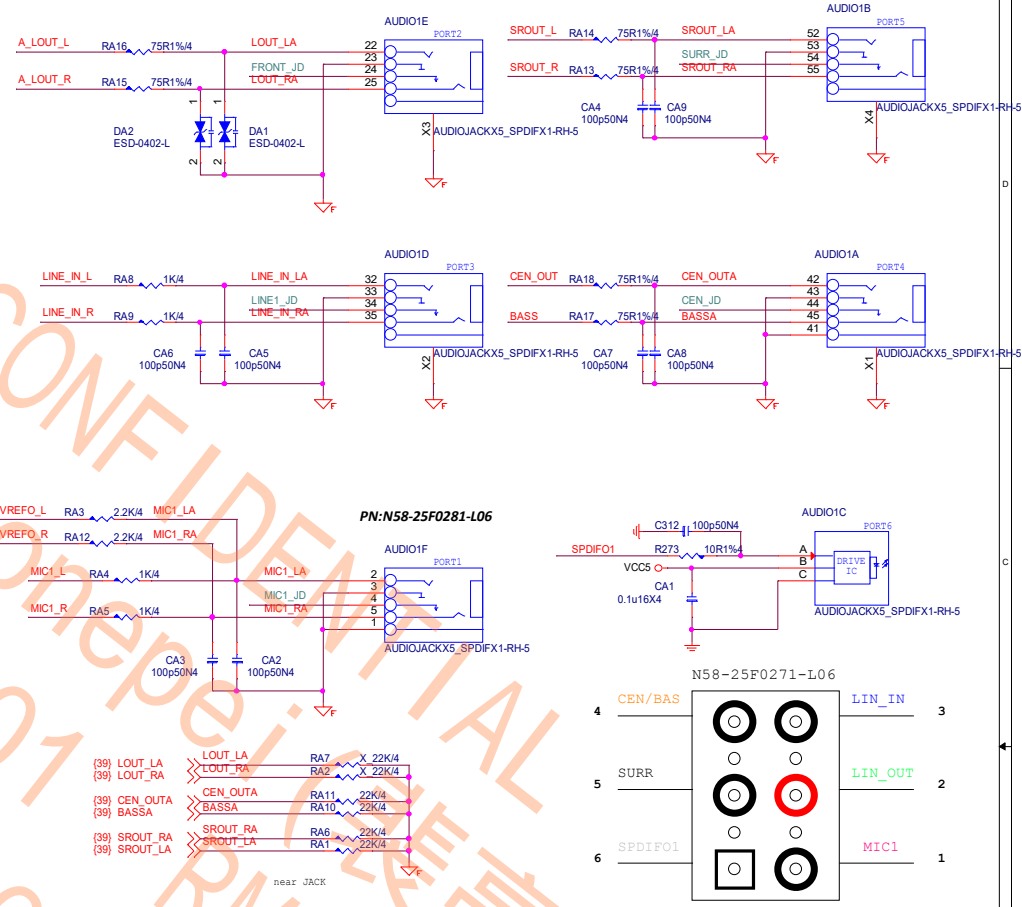
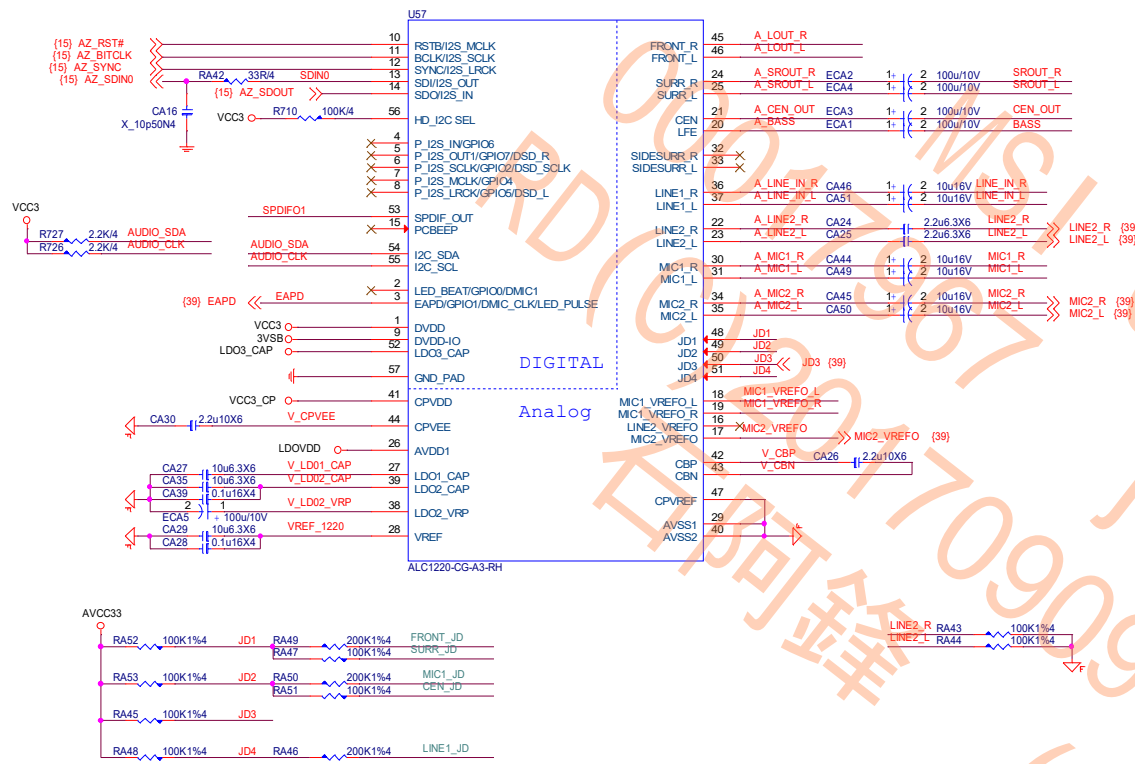
Default Internall pull up 1.65V

Resever For FIX DC or PWM MODE USE By PM SPEC

MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2017090901 RMA工程課
石阿鋒 (00068760)

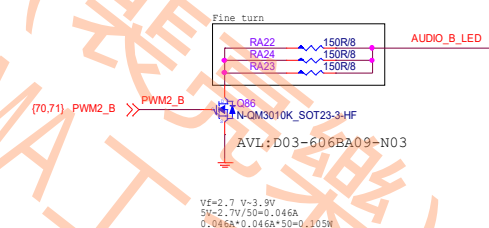
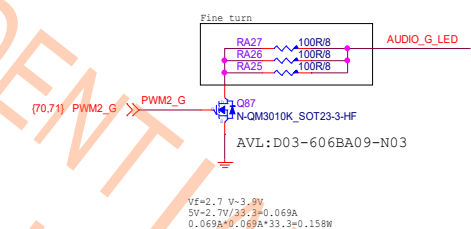
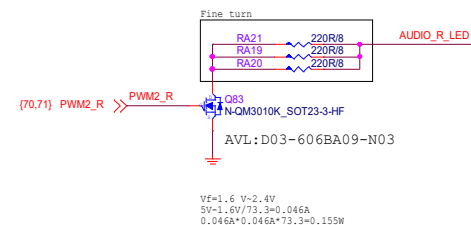
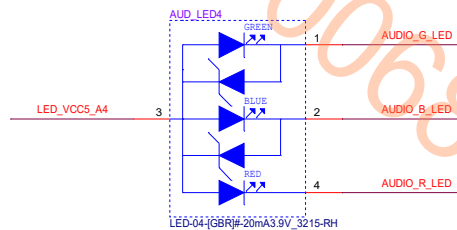
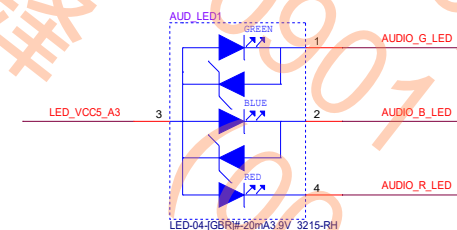
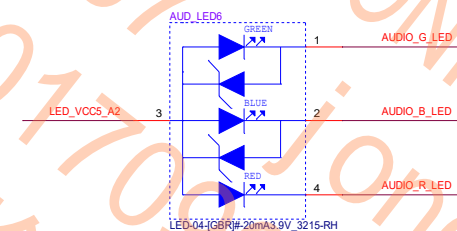
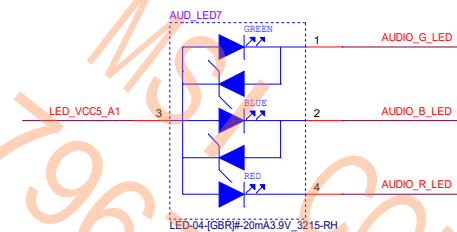
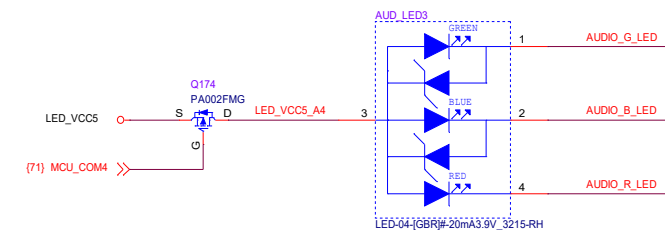
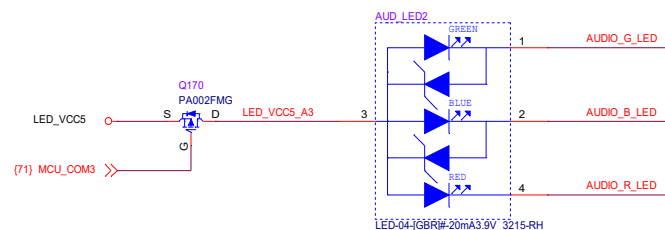
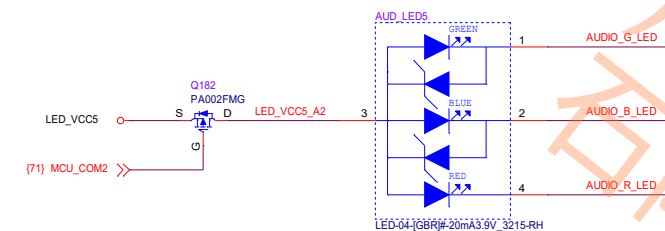
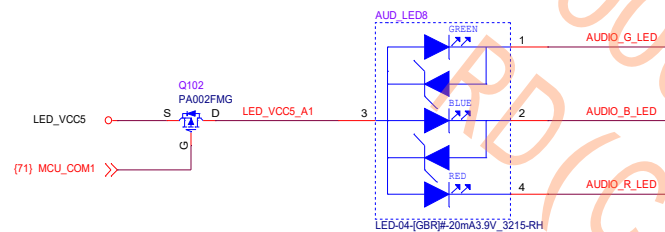
MICRO-STAR INT'L CO.,LTD		
MS-7B06		
Size Custom	Document Description SYSTEM FAN4	Rev 1.2
Date: Wednesday, July 05, 2017		
Sheet 37 of 76		

ALC1220



Audio moat is transparent and width 40mil

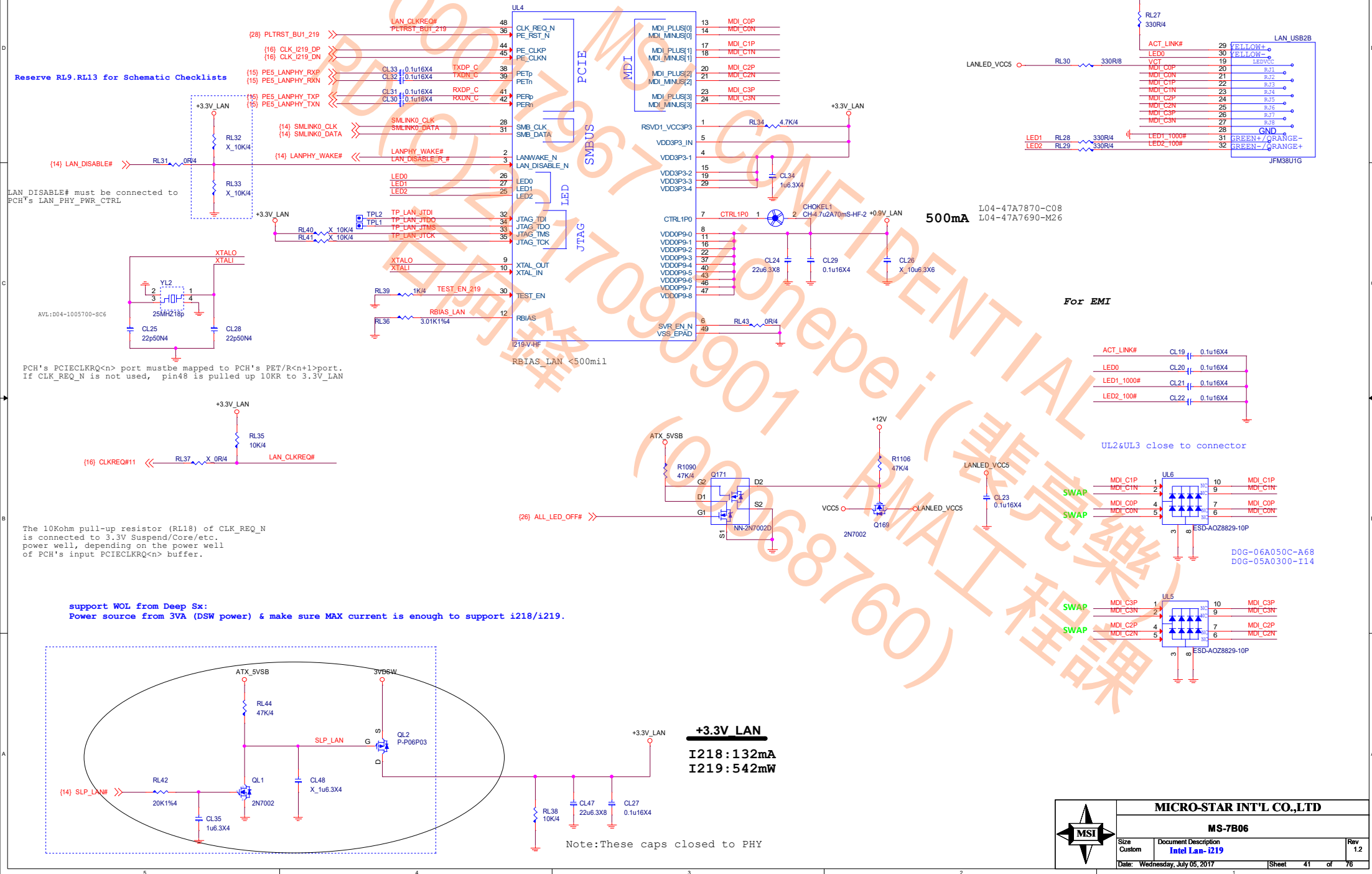
COM1 : LED1/2
COM2 : LED3/4
COM3 : LED5/6
COM4 : LED7/8



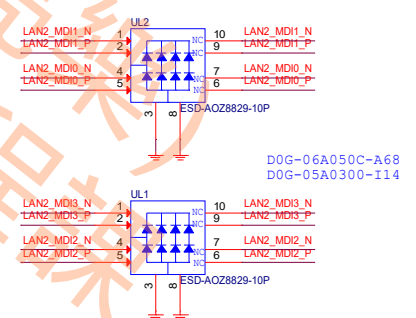
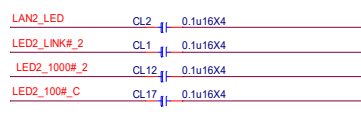
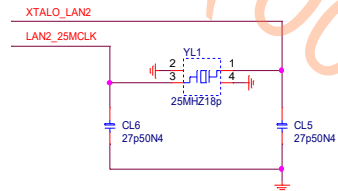
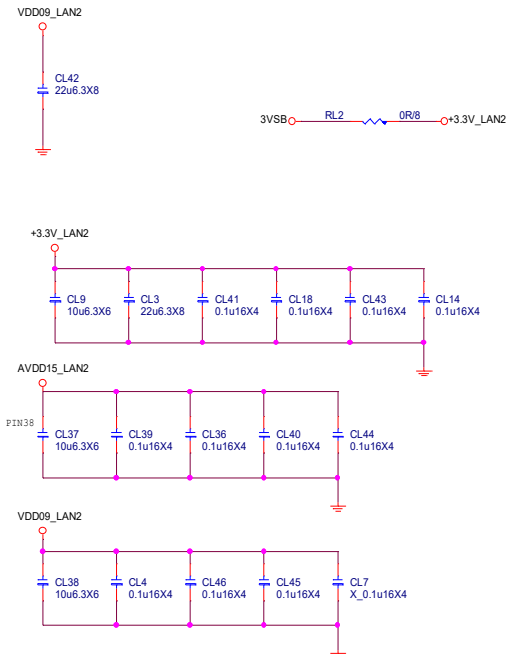
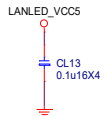
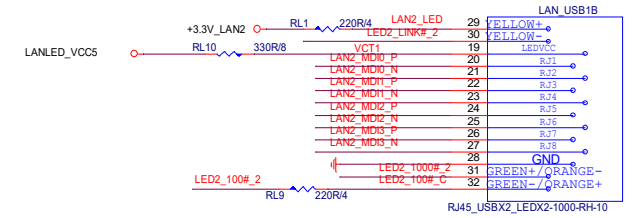
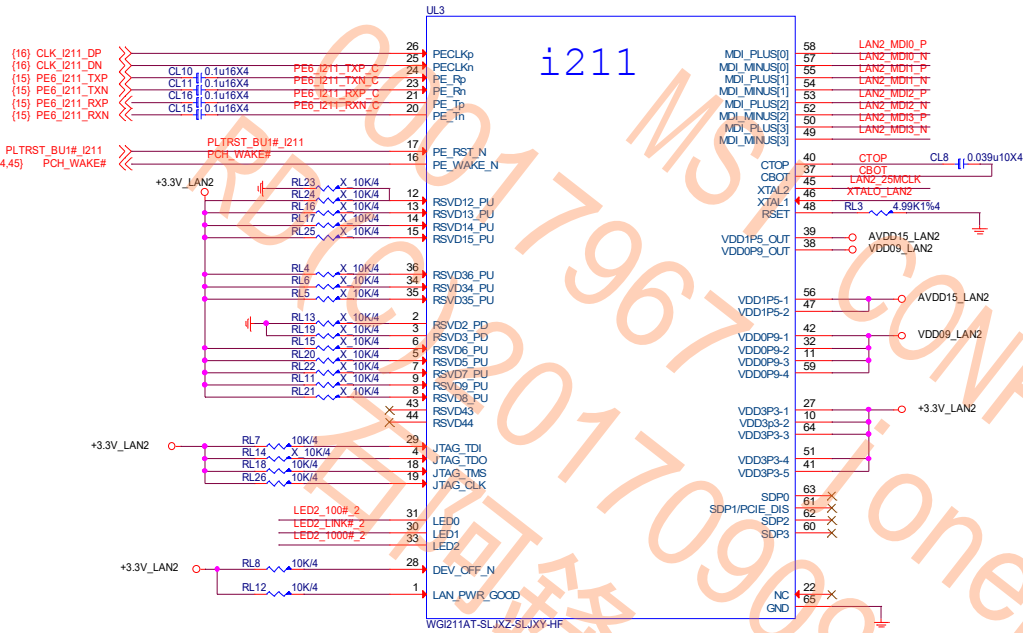
MS-7B06

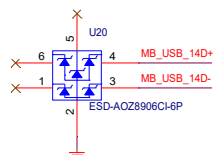
Size Custom	Document Description AUDIO-ACL1220-3	Rev 1.2
Date: Wednesday, July 05, 2017		Sheet 40 of 76

Intel I219V / I218V PHY



LAN2-- I210AT





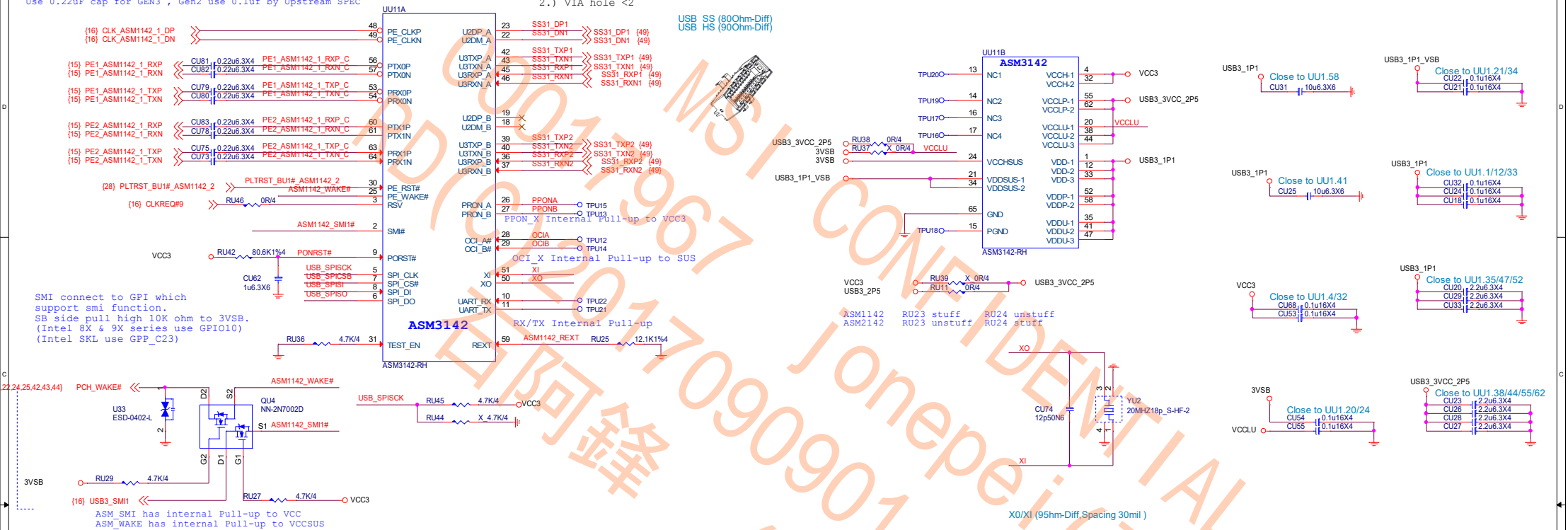
MICRO-STAR INT'L CO.,LTD

MS-7B06

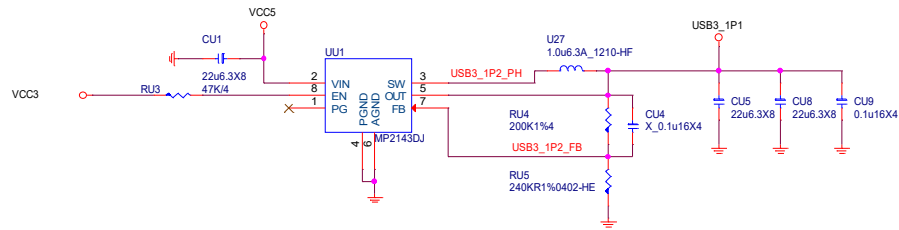
Size Custom	Document Description WIFI BT	Rev 1.2
Date: Wednesday, July 05, 2017		Sheet 43 of 76

Use 0.22uF cap for GEN3 , Gen2 use 0.1uf by Upstream SPEC

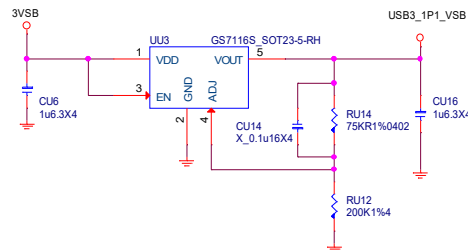
- Layout Guide:
- 1.) USB3.1 to Connector Total Length < 1.5"
 - 2.) VIA hole < 2



ASM3142 1.2 VCC Power

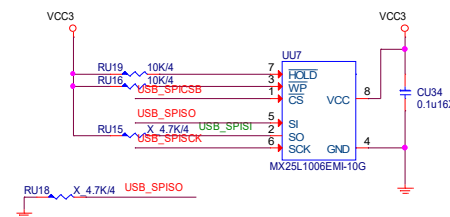


ASM3142 1.2 VSB Power

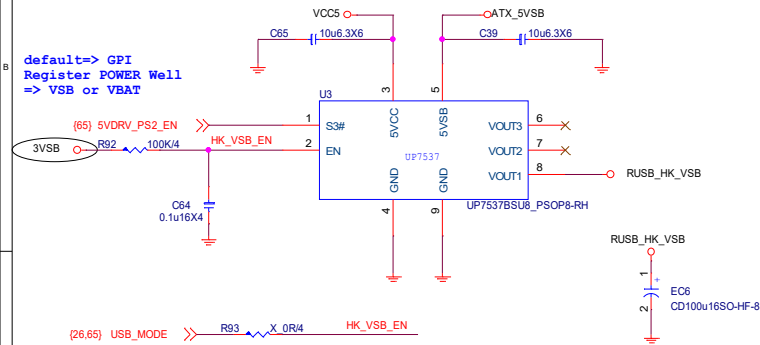
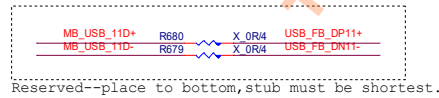
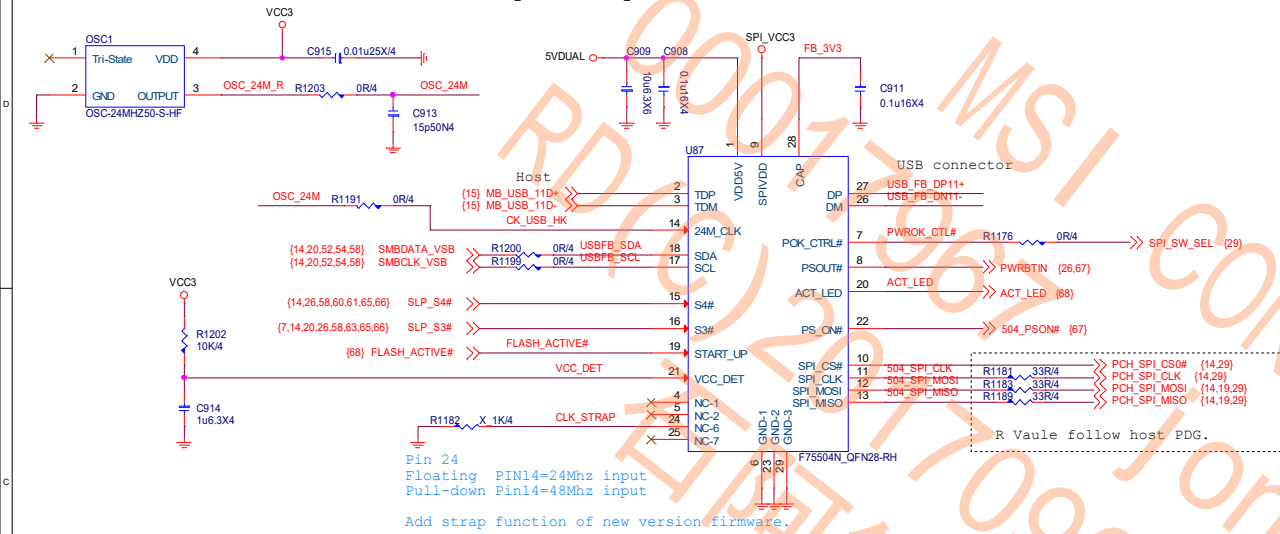


Symbol	Parameter	Power	Min.	Typ	Max.	Unit
USB3.1 Burn in	two USB3.1 Gen-II devices running burn in testing simultaneously	1.05V suspend		TBD		mA
		3.3V normal	1	2.5	4	mA
		3.3V suspend	0.35	0.65	0.9	mA
		2.5V normal	170	200	220	mA
		1.05V normal	390	430	470	mA
USB2.0 Burn in	two USB2.0 devices running burn in testing simultaneously	1.05V suspend	4.5	6	7.5	mA
		3.3V normal	1	2.5	4	mA
		3.3V suspend	5	7	9	mA
		2.5V normal	120	140	160	mA
		1.05V normal	230	260	290	mA
		1.05V suspend	7	8.5	10	mA

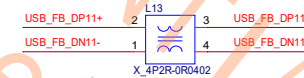
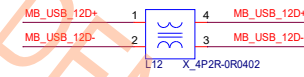
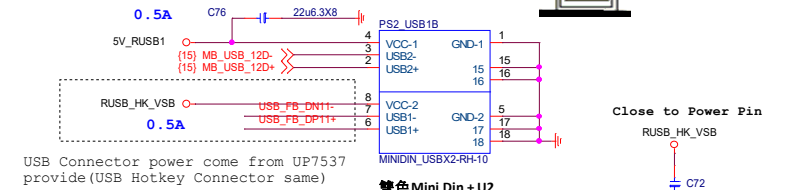
EEPROM



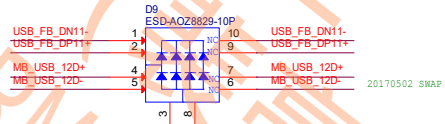
F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.



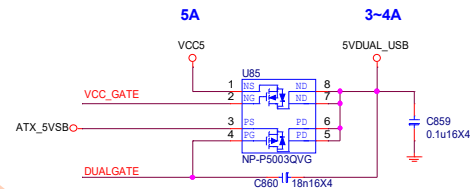
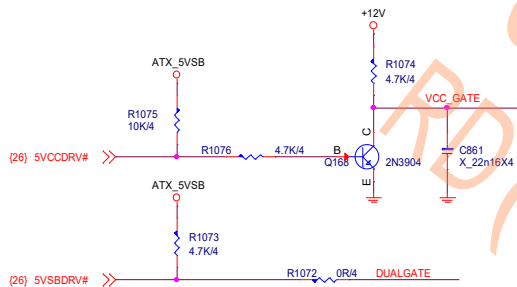
PS2_USB1



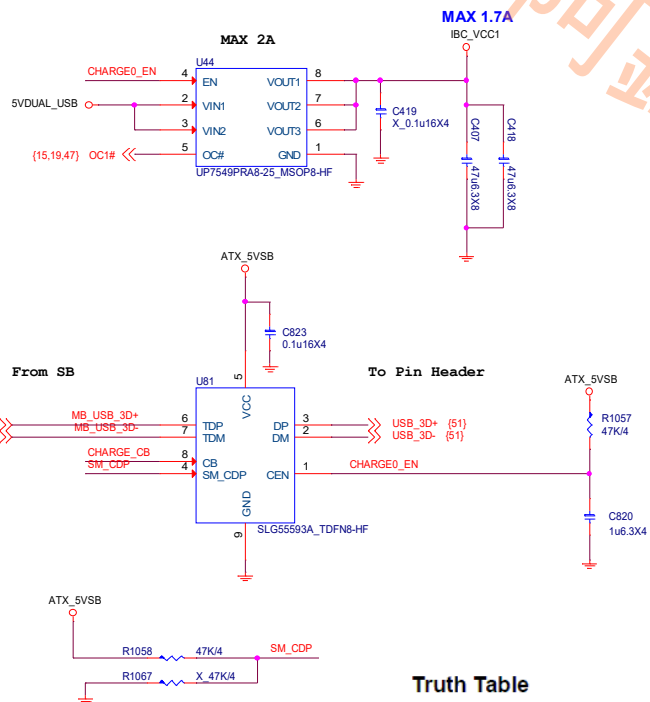
Close to Connector



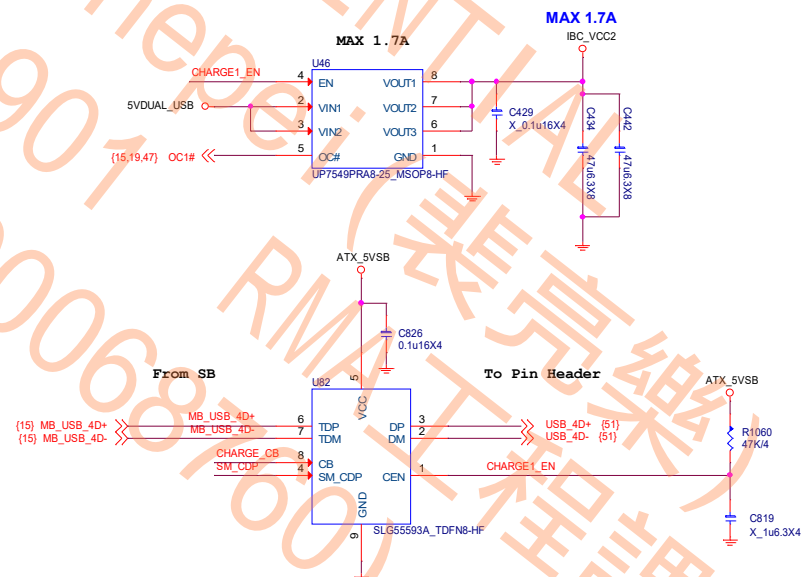
5VDUAL_USB



USB POWER PORT 0 For USB Charging



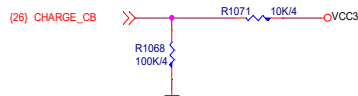
USB POWER PORT 1 For USB Charging



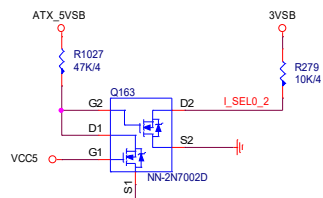
Truth Table

CB	SMART-CDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device) And, when Non-CDP phone is plugged in, the CDP mode will be changed automatically to SDP mode during handshaking protocol for supporting data communication.

Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB



Current Mode

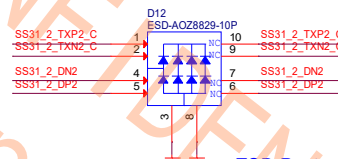
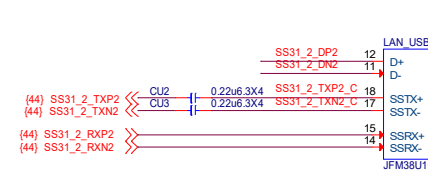
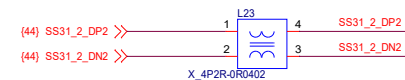
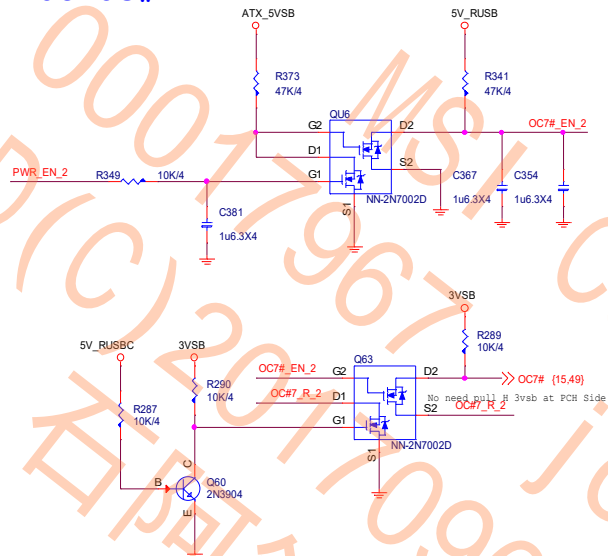


I_SELO : I_SEL1

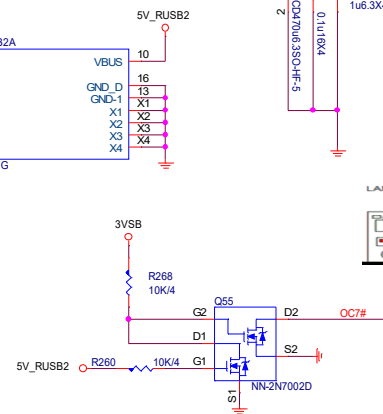
0	X	Default for 900mA
1	0	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode

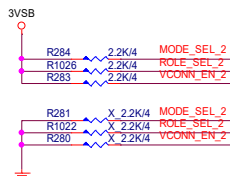
VBUS OC#



ESD Protection
NEAR CONNECTOR



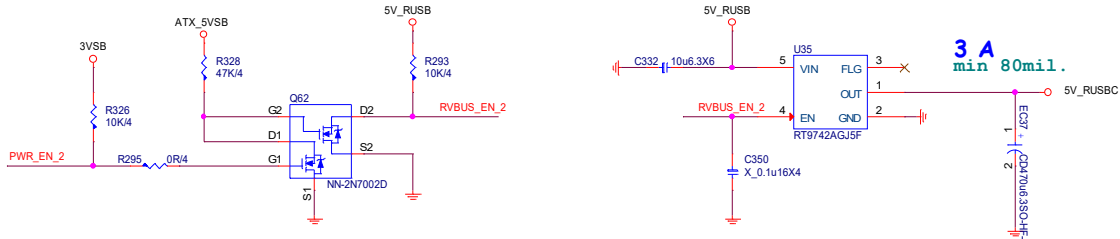
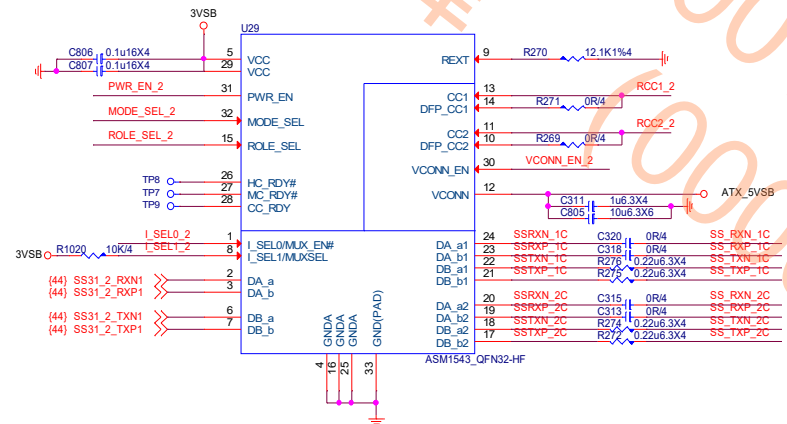
USB Type-C MUX with Configuration Channel (CC)



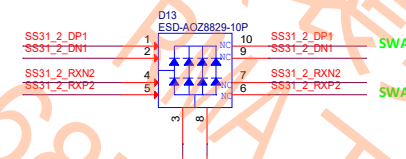
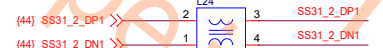
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

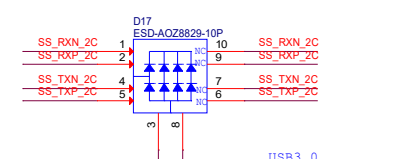
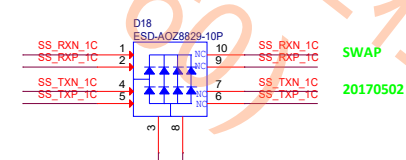
VCONN_EN	
1	enable
0	disable



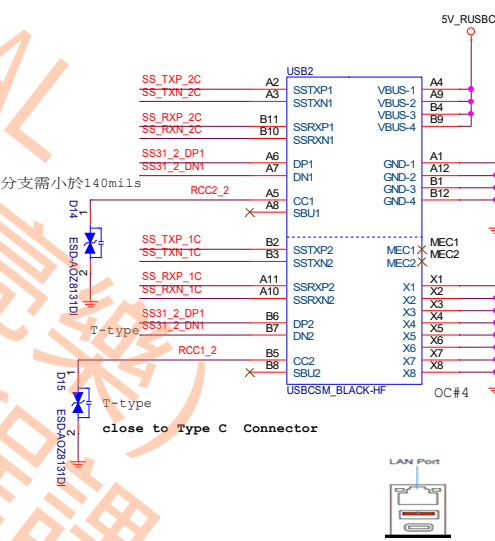
TYPE-C



ESD Protection
NEAR CONNECTOR



USB3.0
D0G-05A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-005 AVL



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MS-7B06			
Size	Document Description	Rev	
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USB 3.1-Type-C

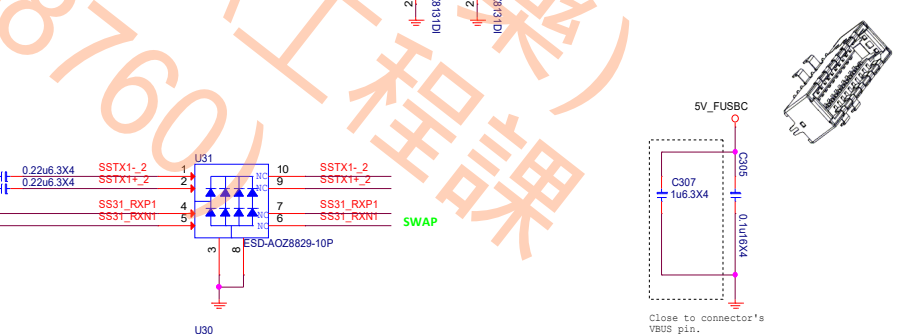
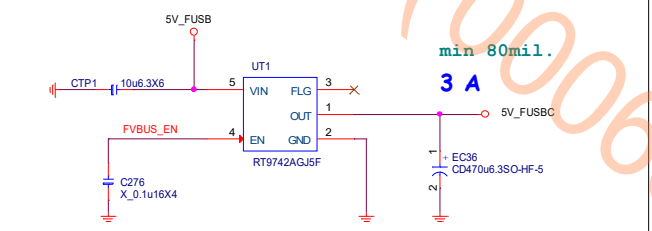
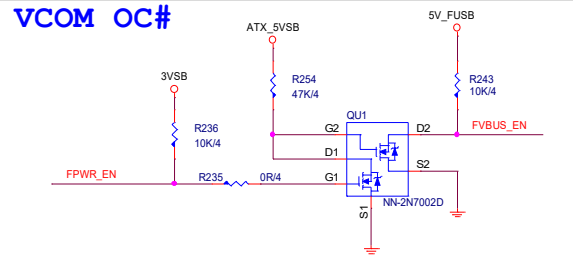
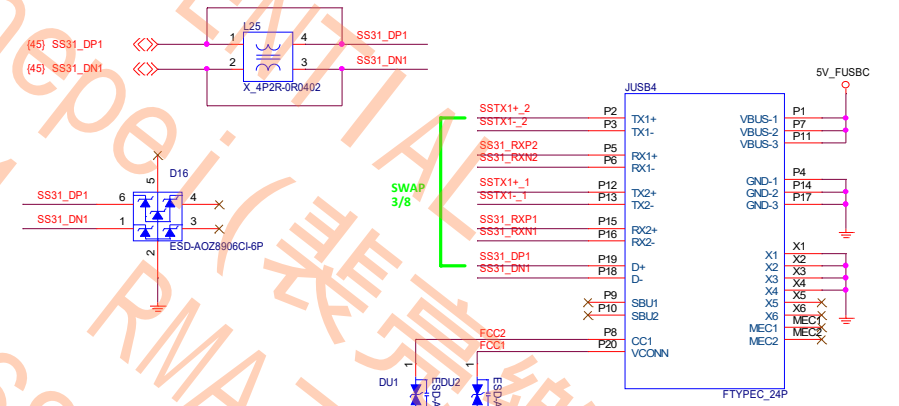
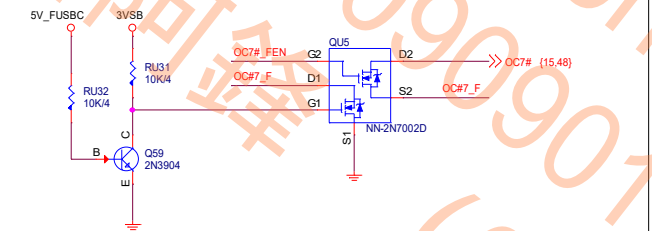
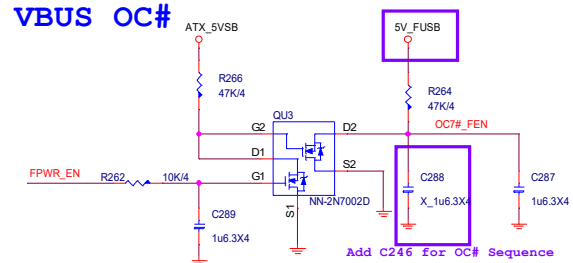
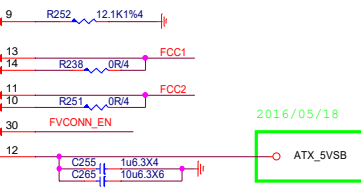
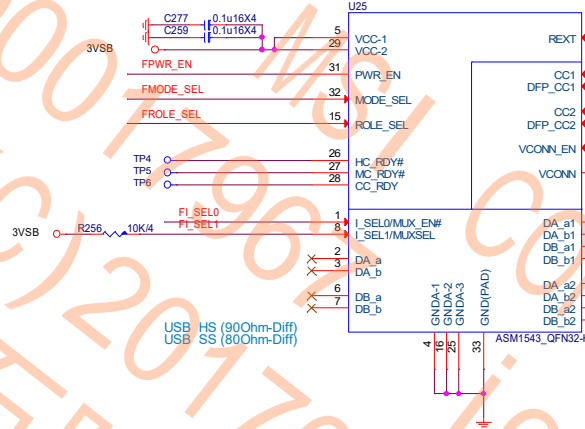
USB Type-C MUX with Configuration Channel (CC)



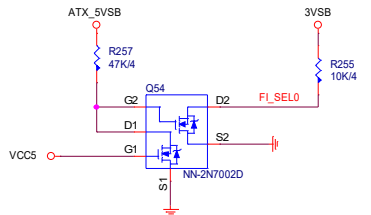
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

VCONN_EN	
1	enable
0	disable

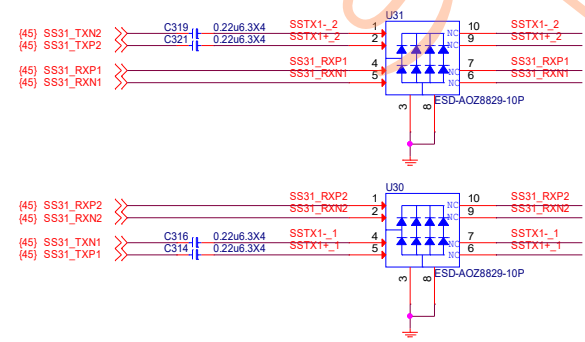


Current Mode



I_SELO: I_SEL1	
X 0	Default for 900mA
0 1	1.5A @5V
1 1	3A @5V

1.5A under S3 mode
3A under S0 mode



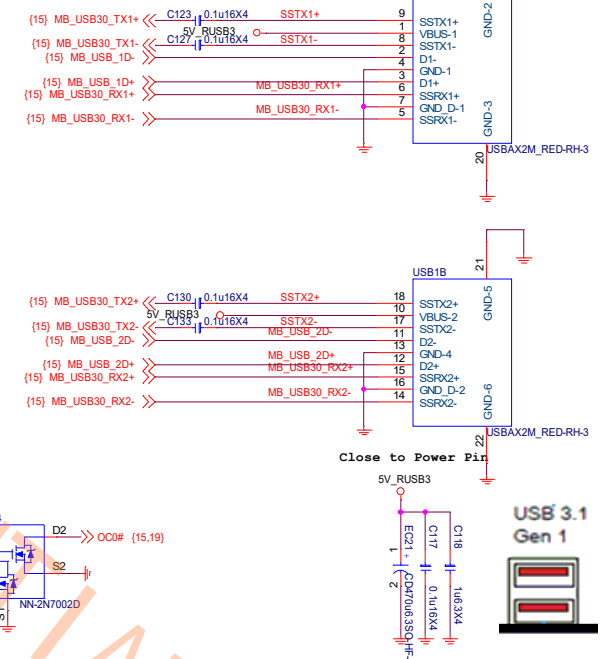
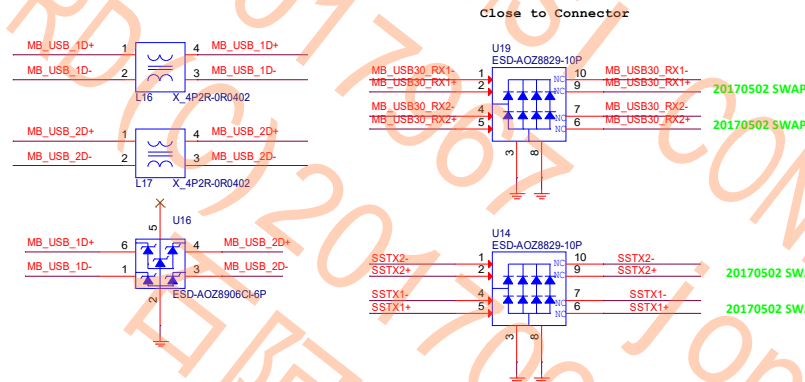
MICRO-STAR INT'L CO.,LTD

MS-7B06

Size Custom Document Description **USB FRONT TYPE-C** Rev 1.2

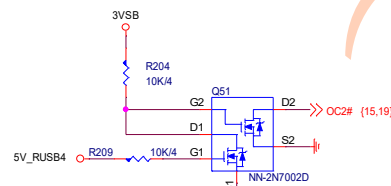
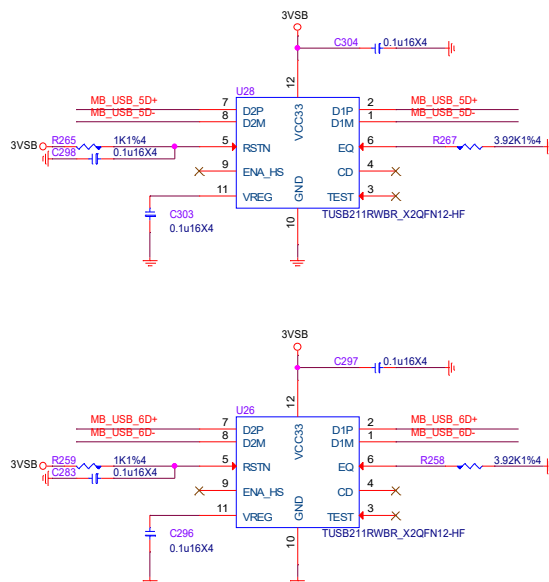
Date: Wednesday, July 05, 2017 Sheet 49 of 76

Close to Connector 1.8A



USB2.0 Redriver

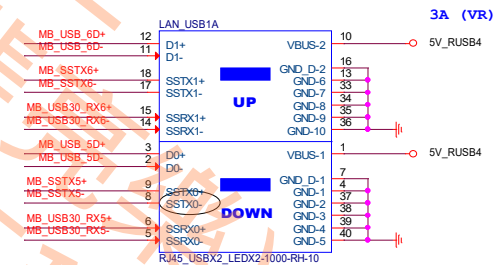
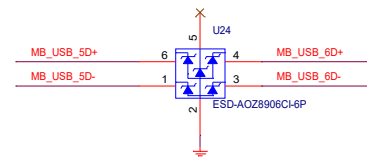
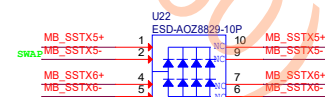
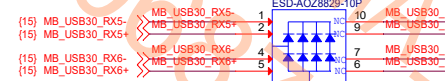
LAN_USB1



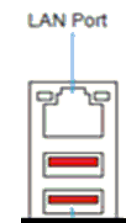
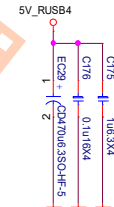
Close to Connector



Close to Connector

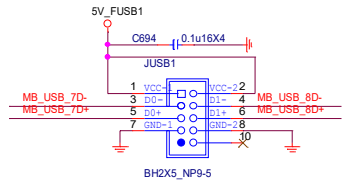
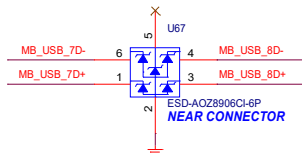
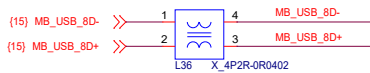
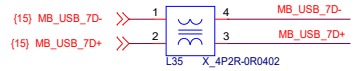


Close to Power Pin

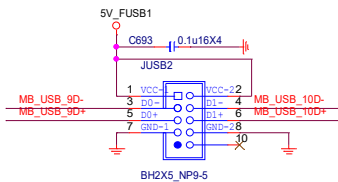
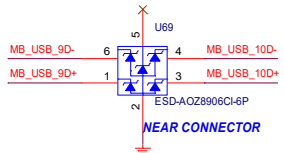
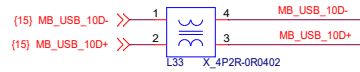
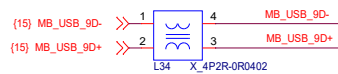


MICRO-STAR INT'L CO.,LTD			
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Size	Custom	Document Description	Rev
		REAR USB CONNECTOR	1.2
Date:	Wednesday, July 05, 2017	Sheet	50 of 76

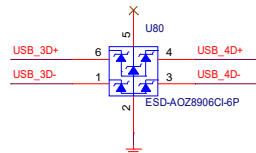
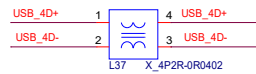
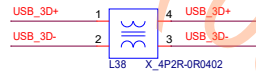
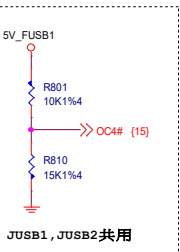
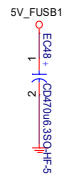
FRONT USB PORT 7,8



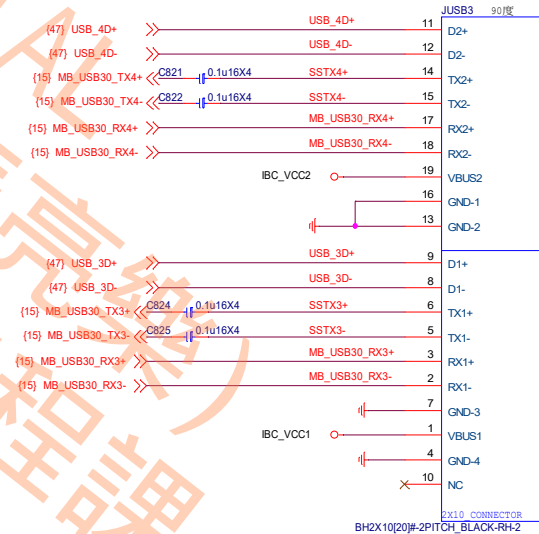
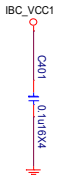
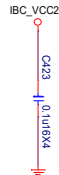
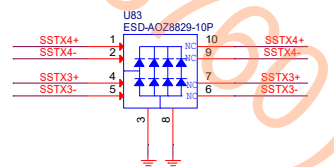
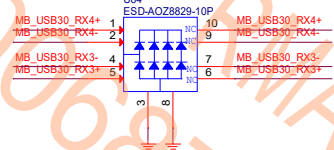
FRONT USB PORT 9,10



Close to JUSB2

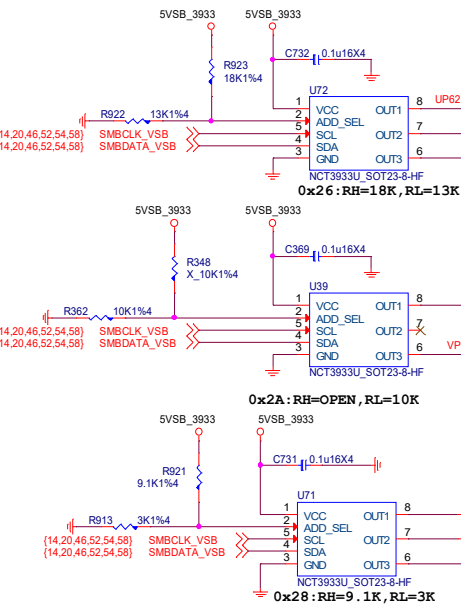


Close to Connector



MICRO-STAR INT'L CO.,LTD			
MS-7B06			
Size	Document Description	Rev	
Custom	Rear/Front USB2.0	1.2	
Date:	Wednesday, July 05, 2017	Sheet	51 of 76

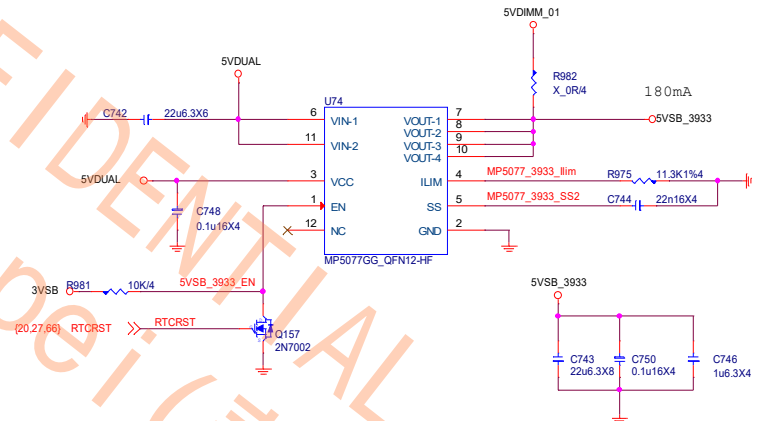
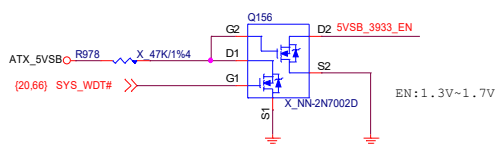
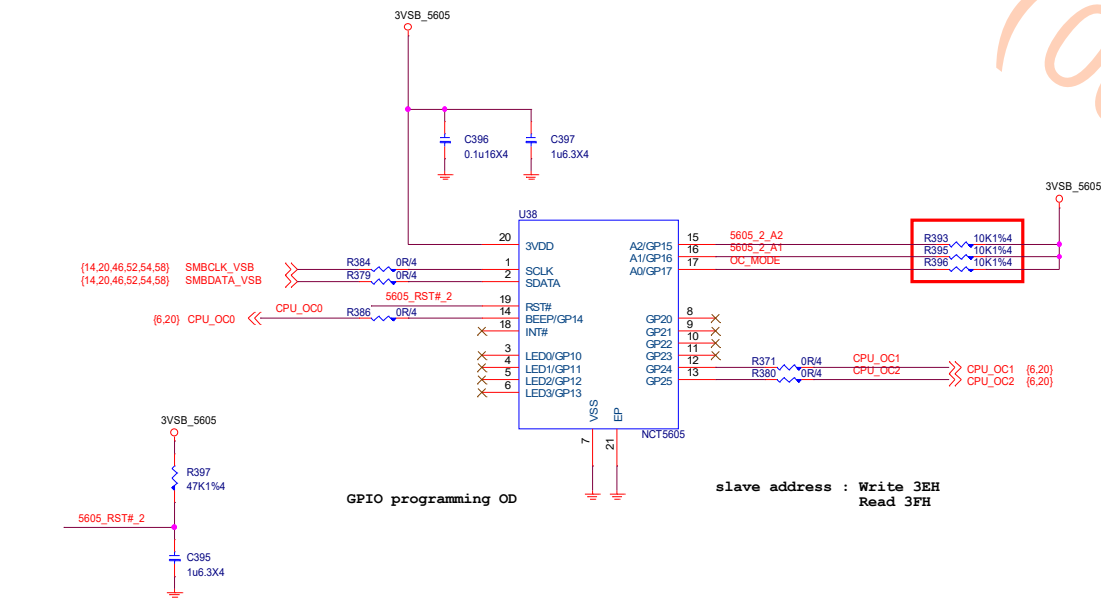
UPI VOLTAGE CONSOLE

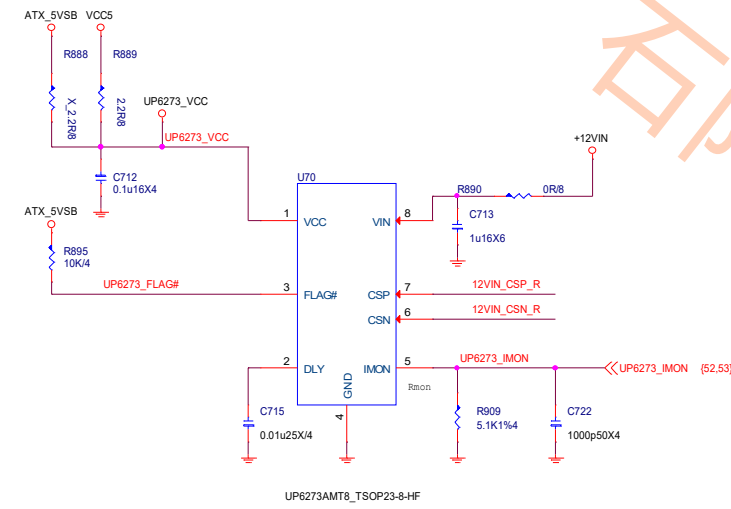
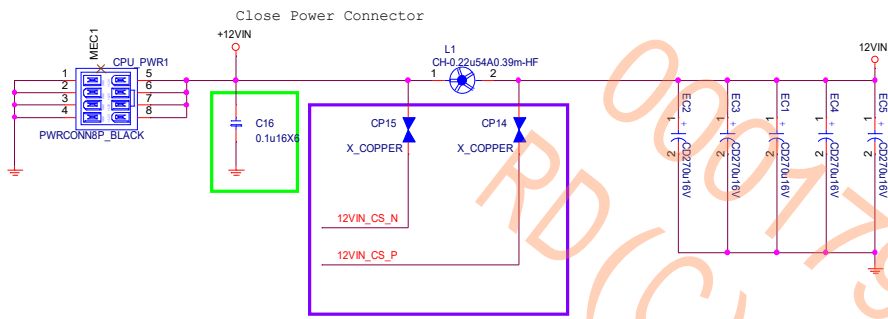


VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.2	3	3.9	OPEN
BUS_SEL	0%	25%	42%	58%	75%	100%

RSVD FOR OC





$I_{in} = (V_{mon} \cdot R_{csn}) / (R_{mon} \cdot R_{dc})$

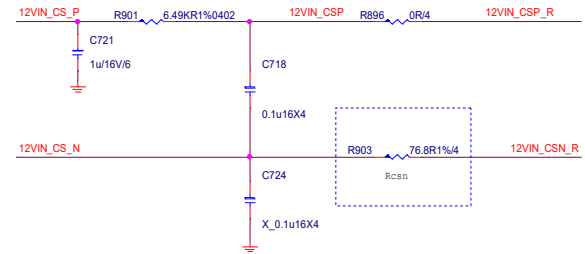
$V_{mon} = 1.2$

can change OCP trigger level by Rcsn and Rmon

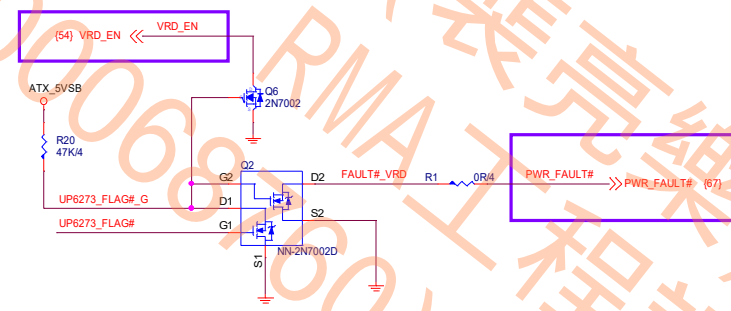
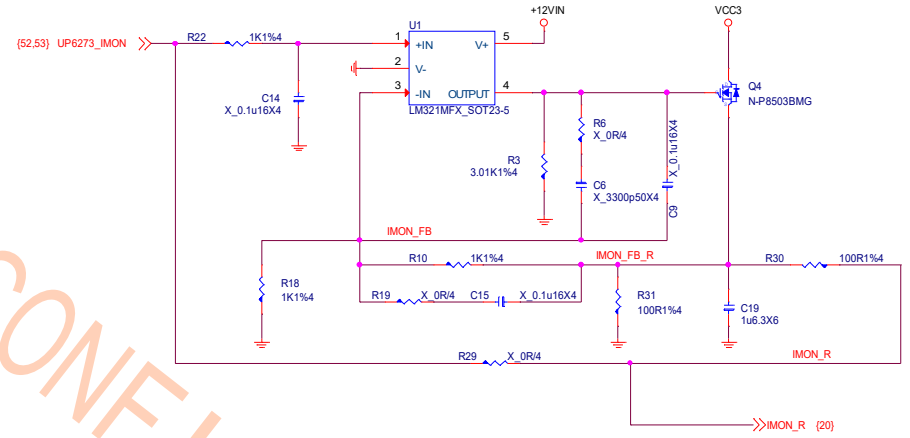
$0.7 \cdot OCP \cdot 400A \cdot 1.8V = 90\% \cdot 12 \cdot I$

$I = 46.6 A$

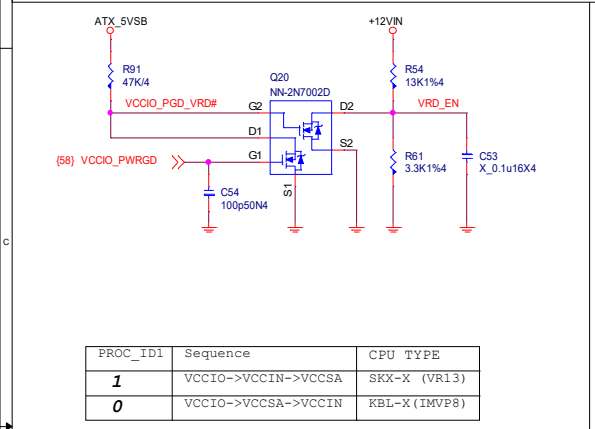
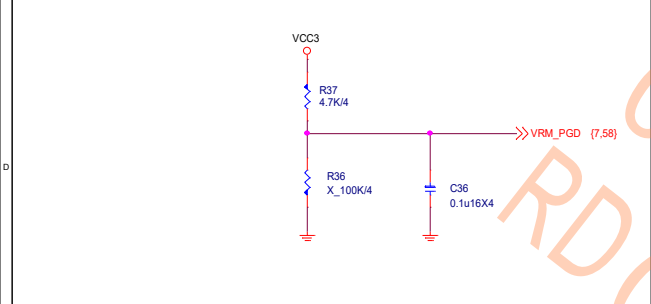
— 0.7A
Rmon=5.18ohm
Rcsn=0.0768Kohm
DCR=0.39mohm
Vmon=1.2V
Iocp=46.33484163A



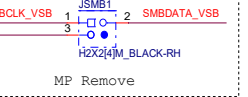
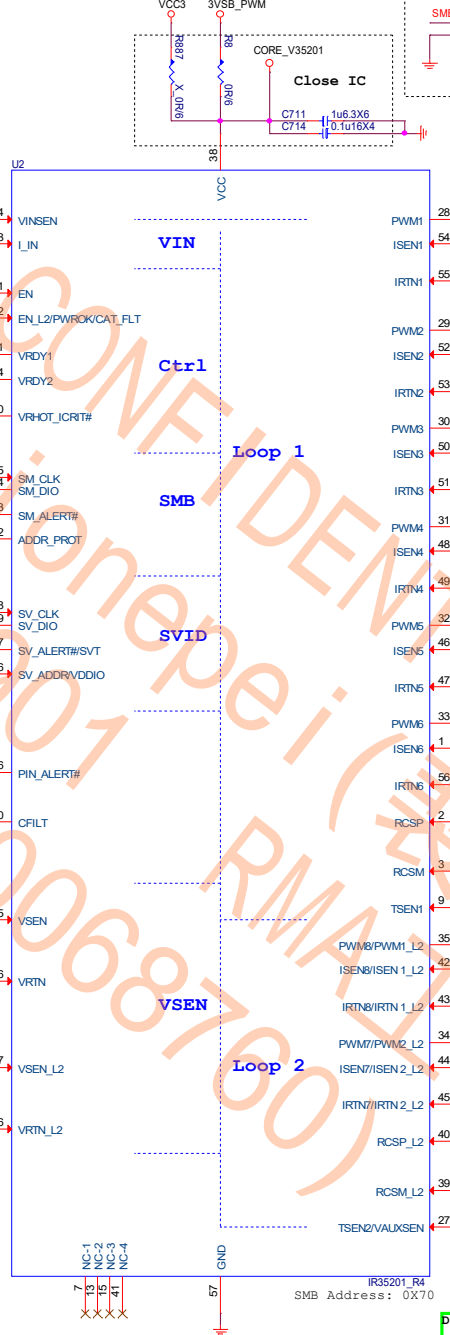
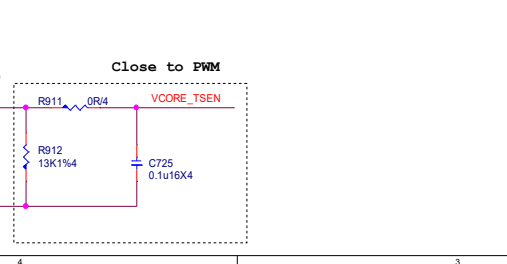
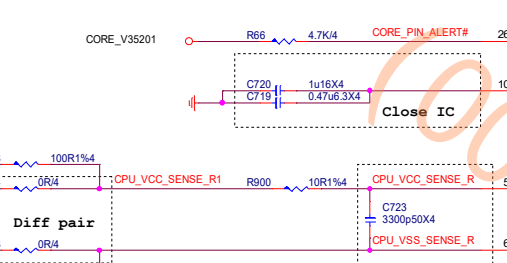
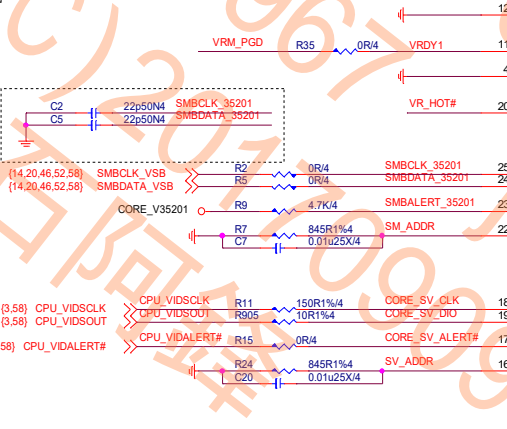
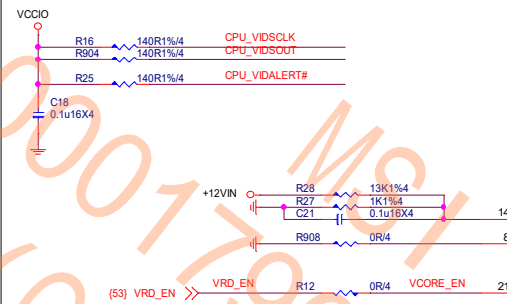
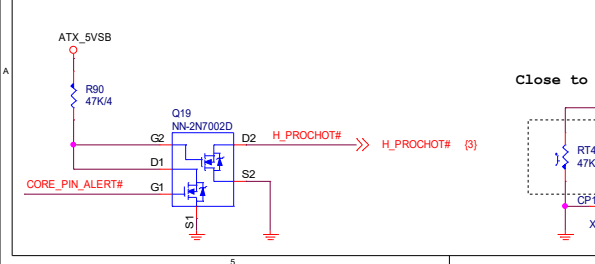
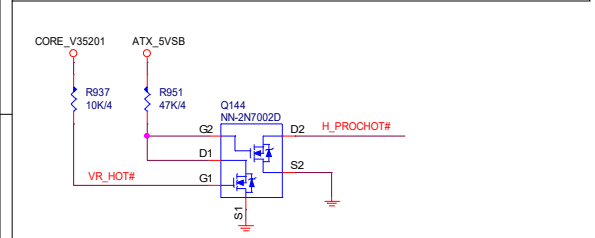
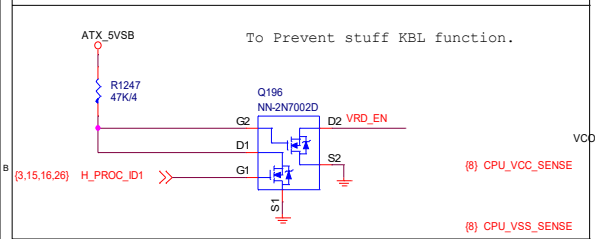
Near PWM IC



VRMPWRGD LEVEL SHIFT

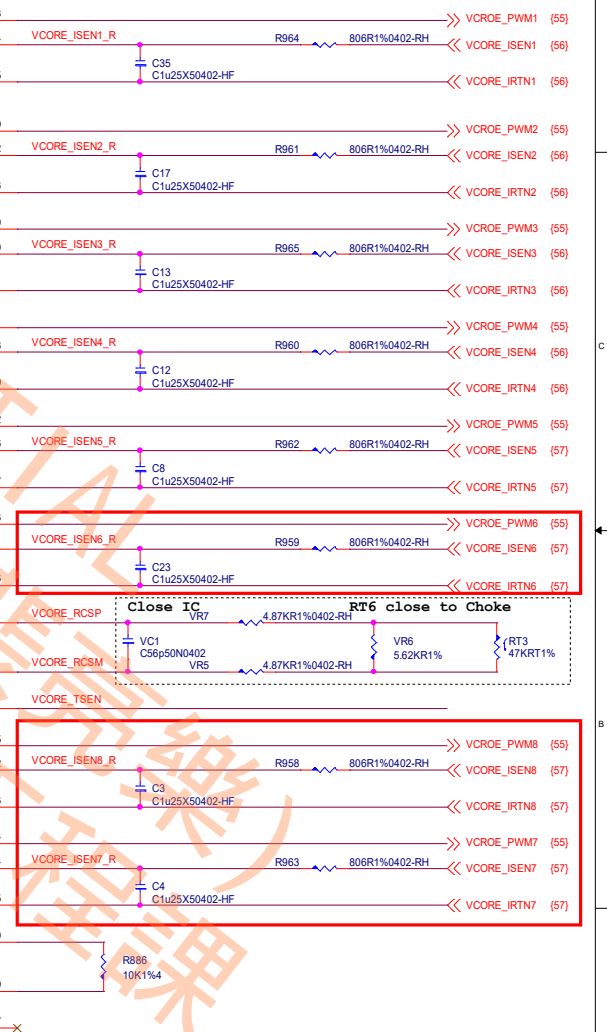


PROC_ID1	Sequence	CPU TYPE
1	VCCIO->VCCIN->VCCSA	SKX-X (VR13)
0	VCCIO->VCCSA->VCCIN	KBL-X (IMVP8)



Vcore: ICC Max
100A
LL: 1.0 mohm
OCP: 400A

VSA: ICC
Max 15A
OCP: 40A



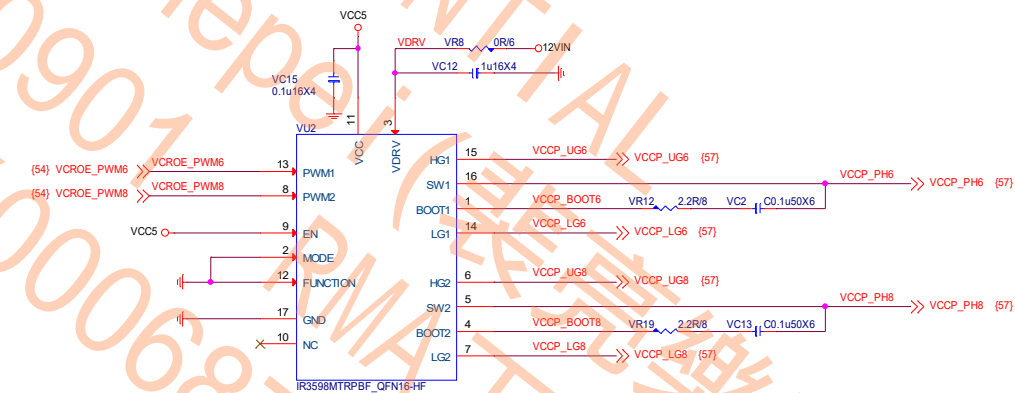
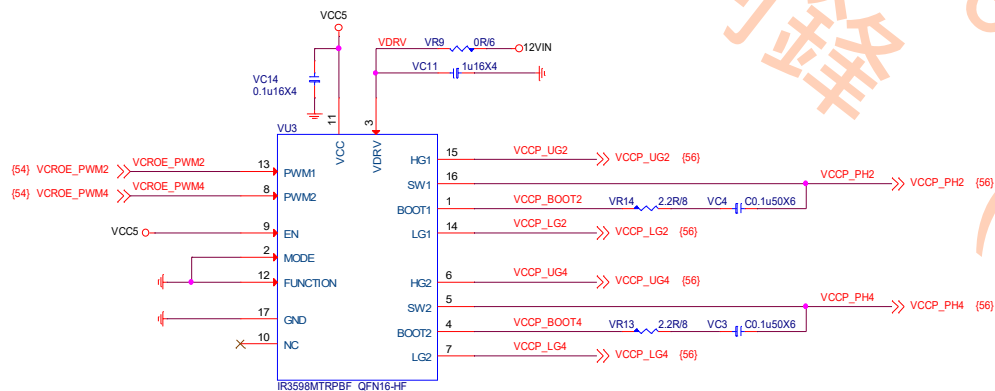
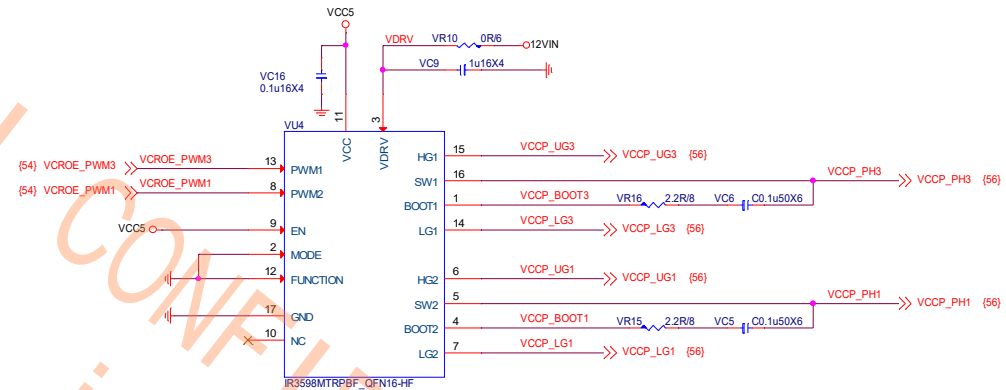
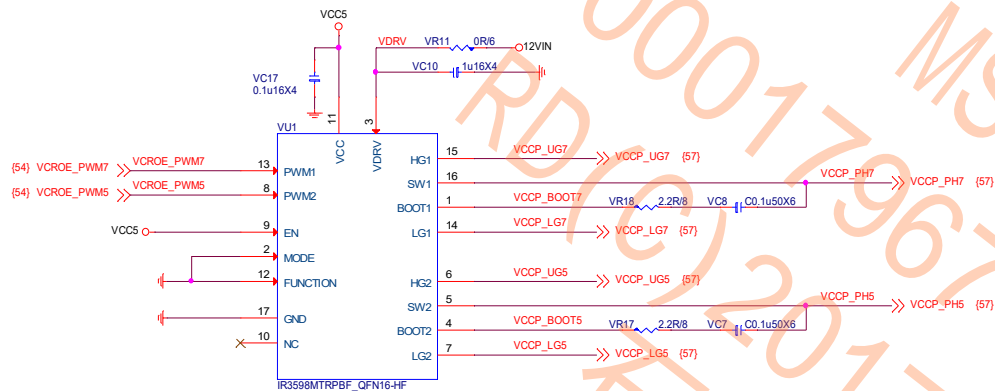
	VR53	VR54	VC20	VR58	VR57	VR59	VR60
Temp	6.49k	10k	100p	X	0R	X	0R
VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

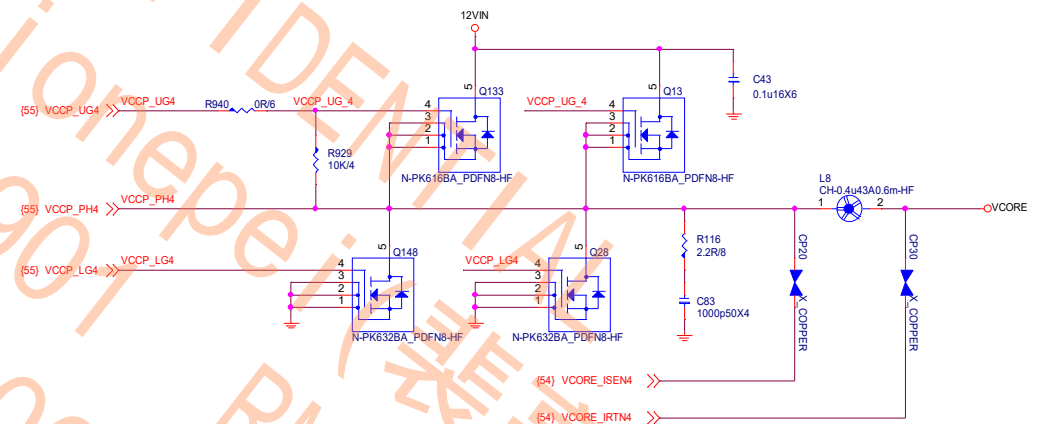
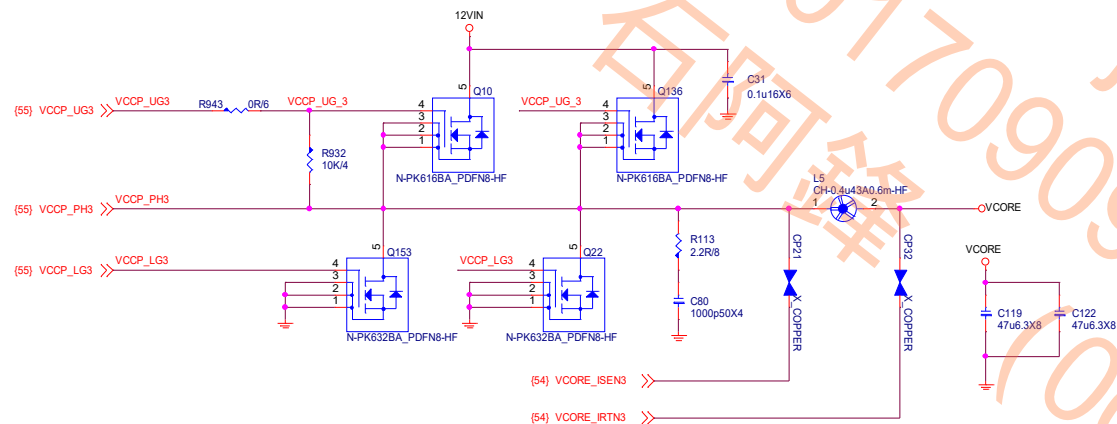
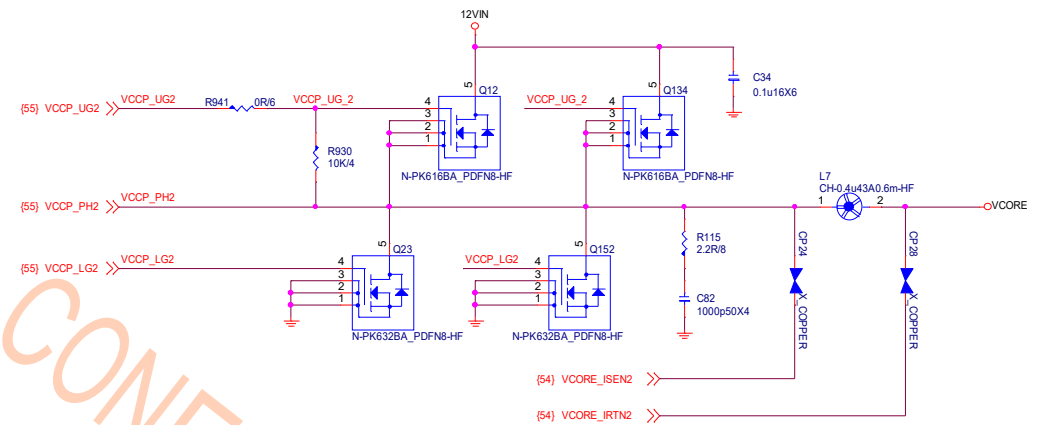
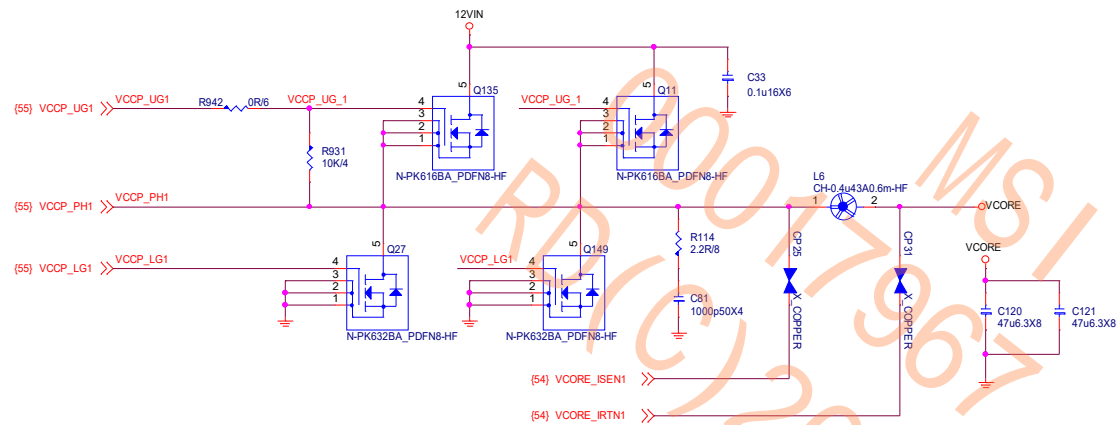
MICRO-STAR INT'L CO.,LTD

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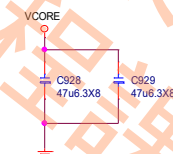
Size Custom Document Description **CPU PWR-IR35201** Rev 1.2

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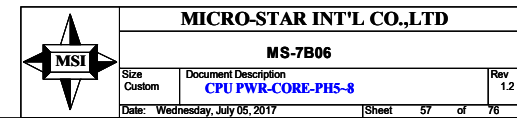
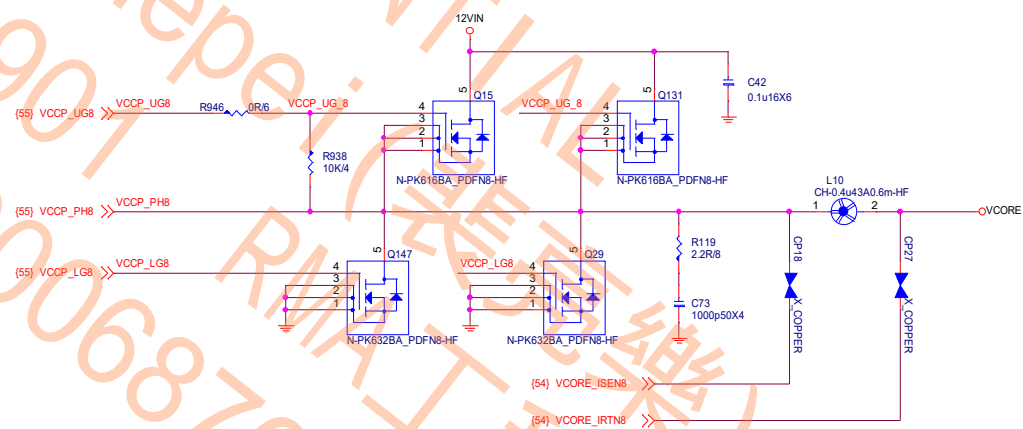
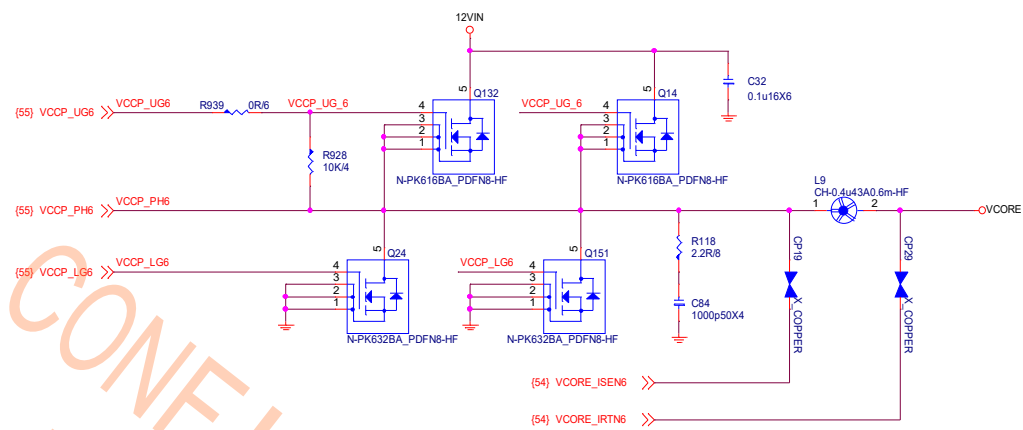
Dedensive design

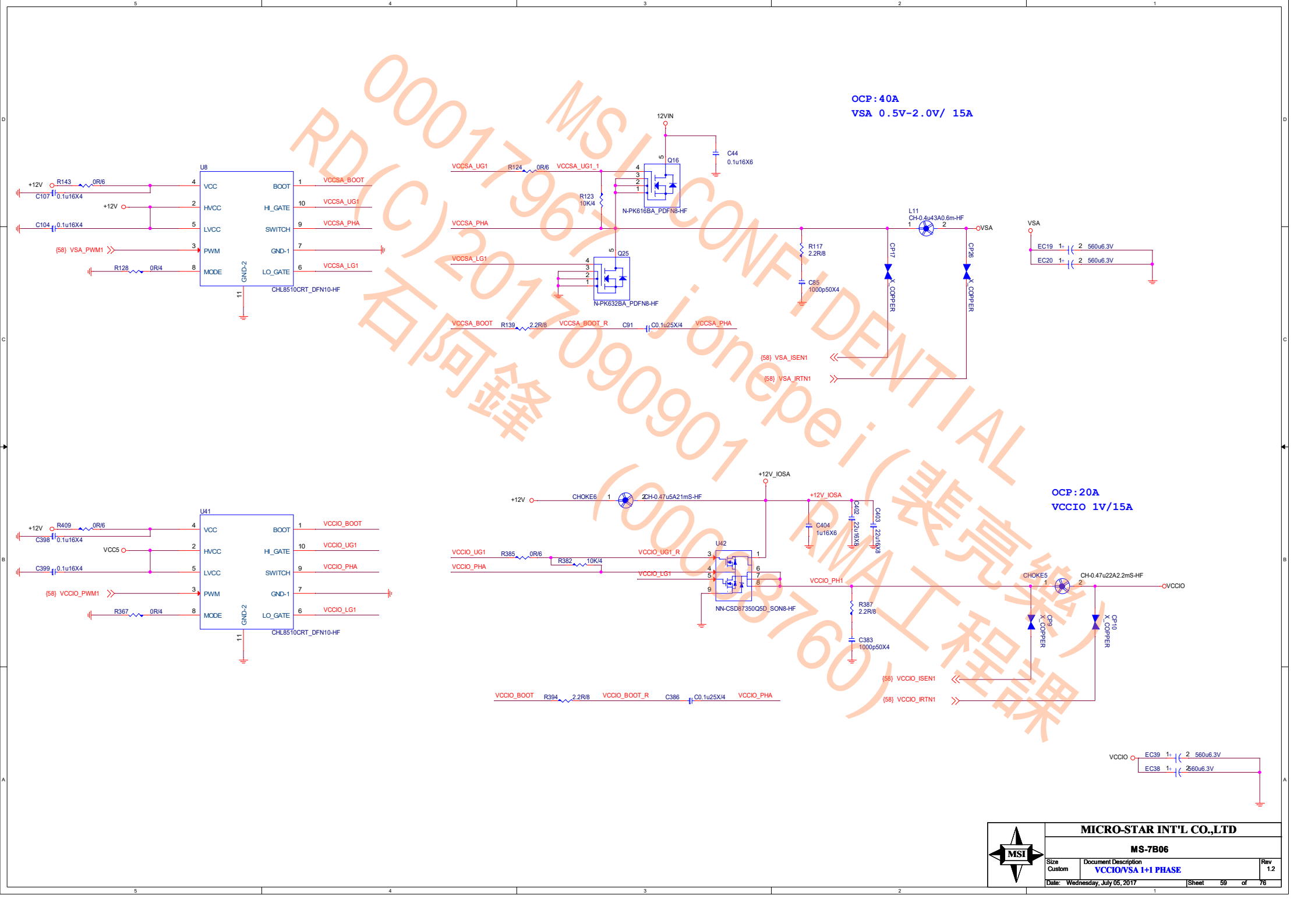


MICRO-STAR INT'L CO.,LTD

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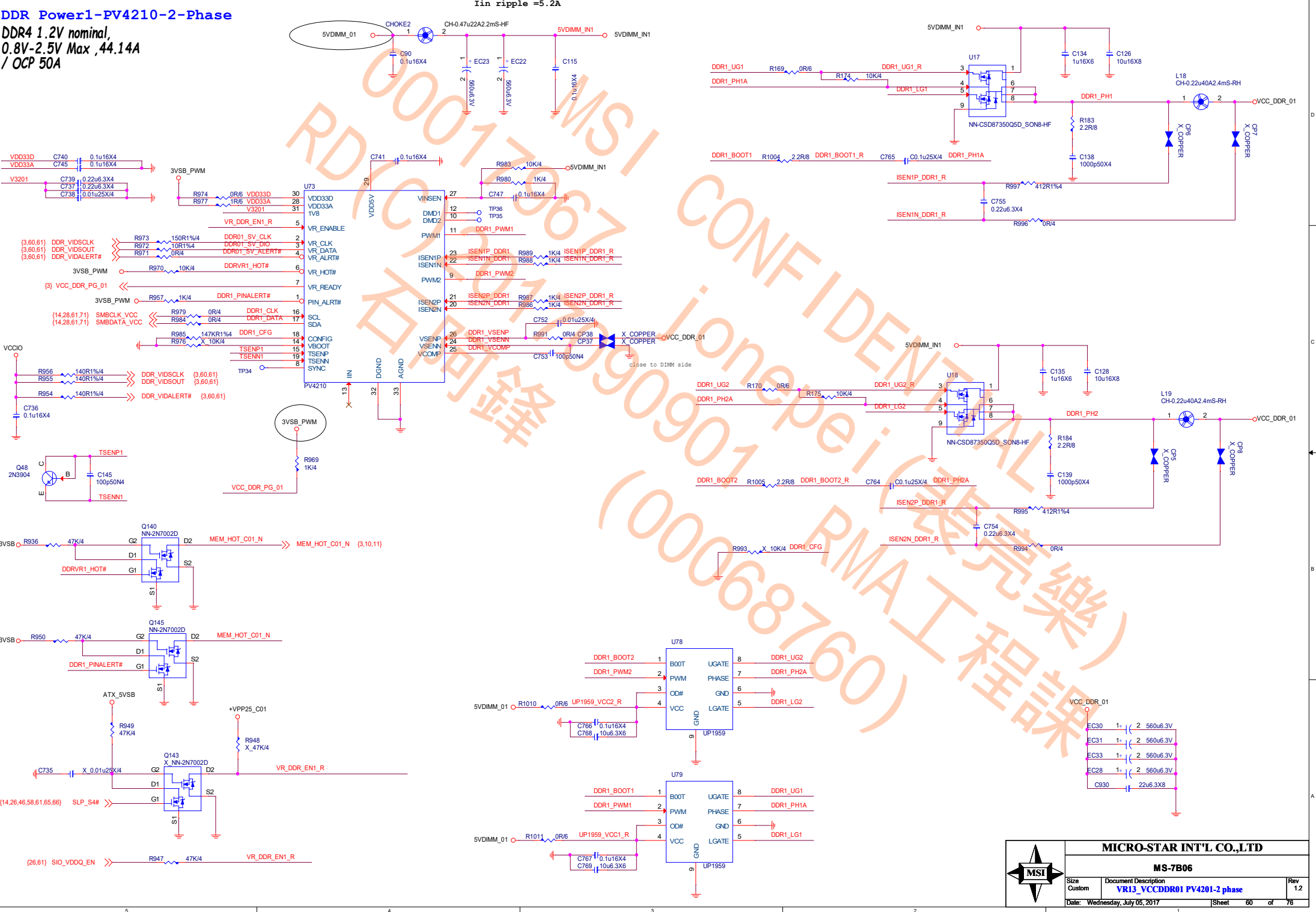
Size	Document Description	Rev
Custom	CPU PWR-CORE-PH1-4	1.2
Date: Wednesday, July 05, 2017	Sheet 56 of 76	





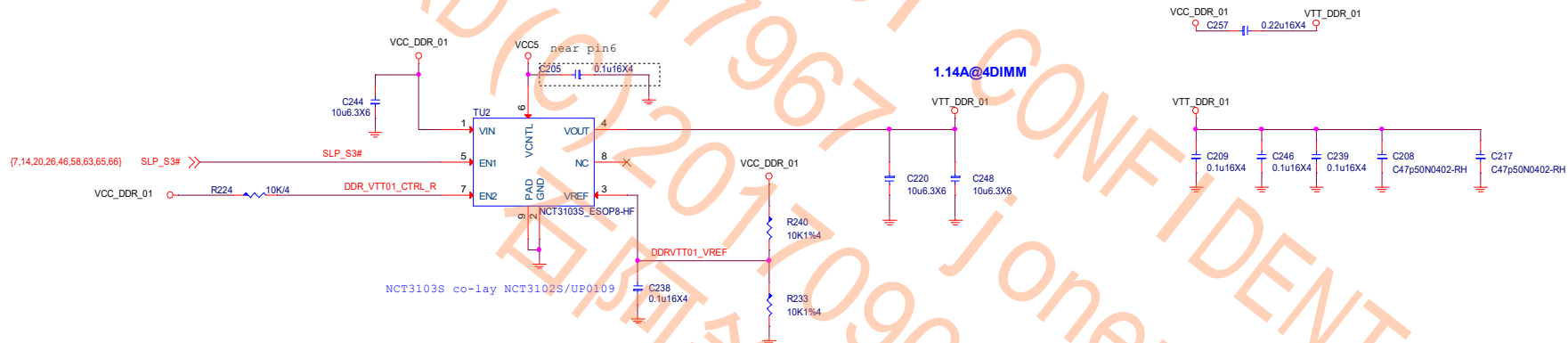
DDR Power1-PV4210-2-Phase

DDR4 1.2V nominal,
0.8V-2.5V Max ,44.14A
/ OCP 50A



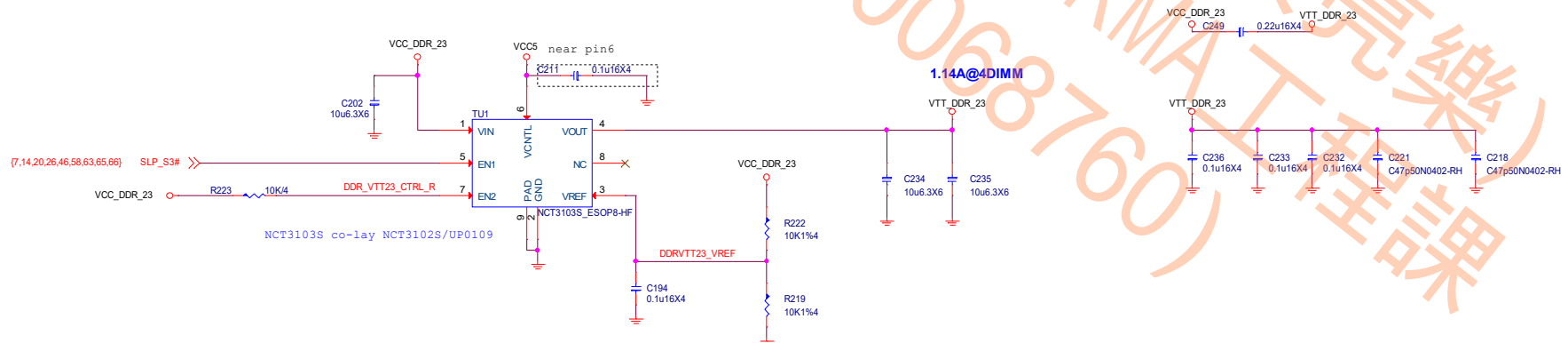
DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

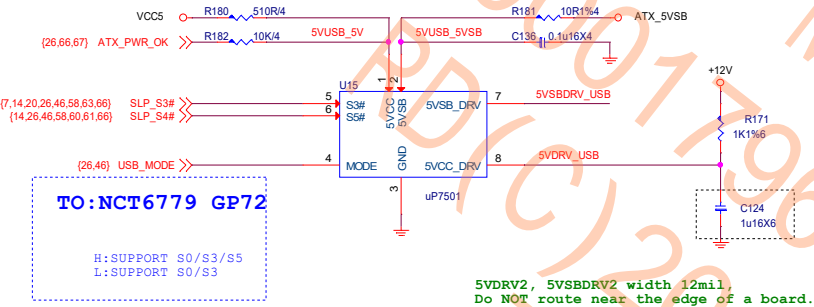


MICRO-STAR INT'L CO.,LTD

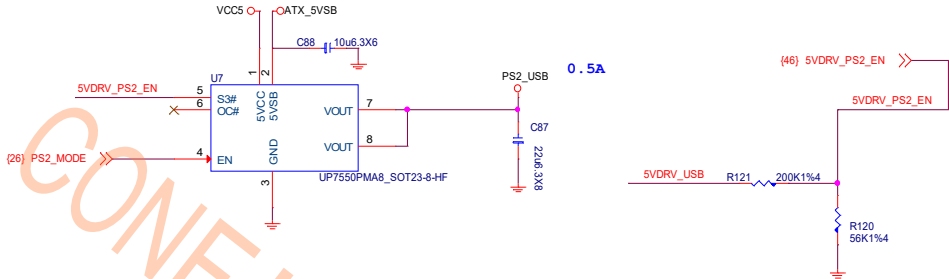
MS-7B06

Size Custom	Document Description VTTDDR	Rev 1.2
Date: Wednesday, July 05, 2017	Sheet 63 of 76	

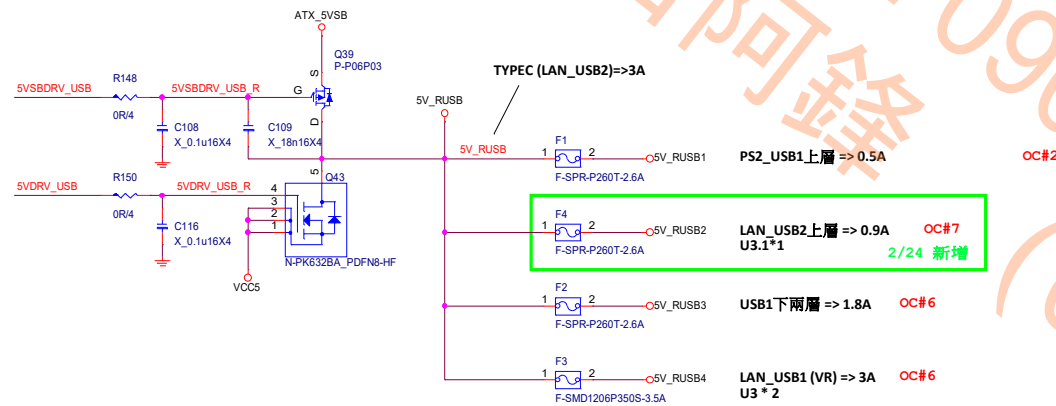
USB POWER



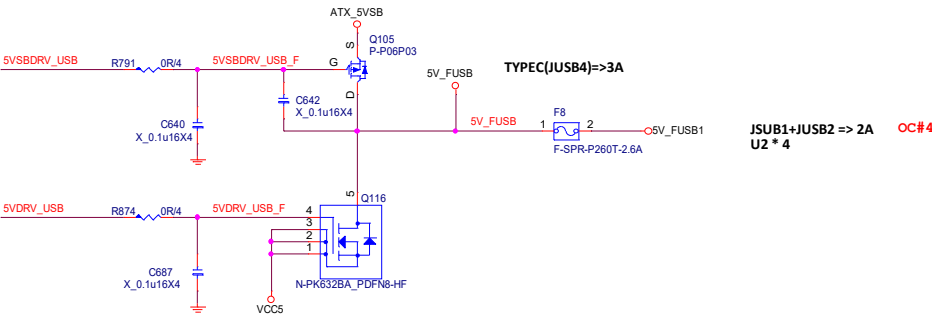
PS2 POWER



REAR USB PORT POWER



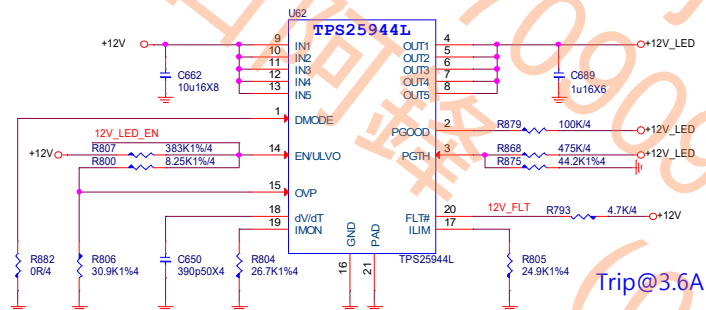
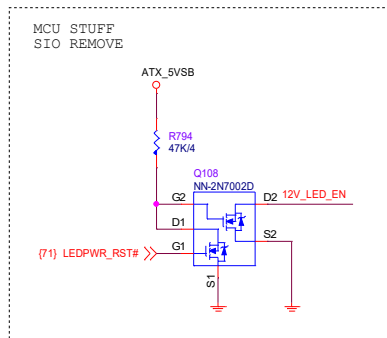
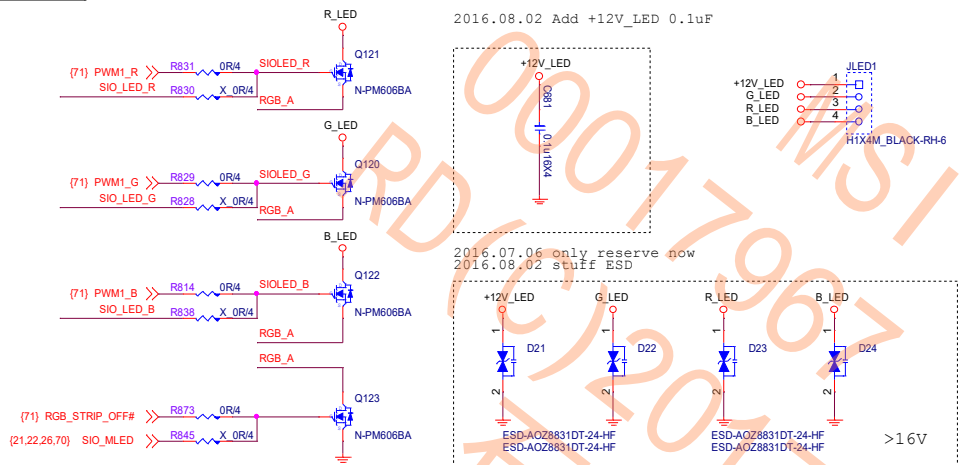
FRONT USB PORT POWER



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Size Custom	Document Description USB Power		Rev 1.2
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LED STRIPLINE



RGB LED defult setting

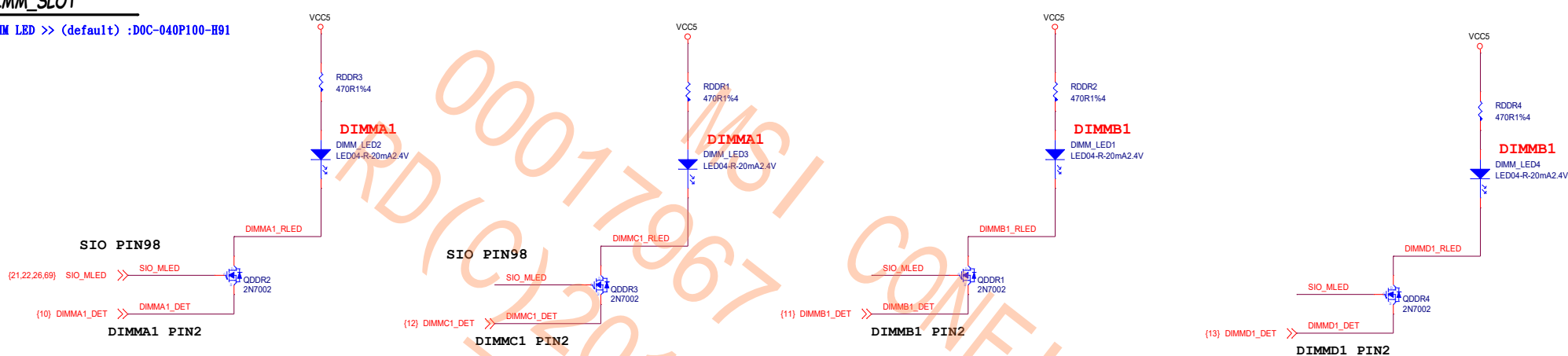
(26) SIO_LED_R >> SIO_LED_R
(26) SIO_LED_G >> SIO_LED_G
(26) SIO_LED_B >> SIO_LED_B



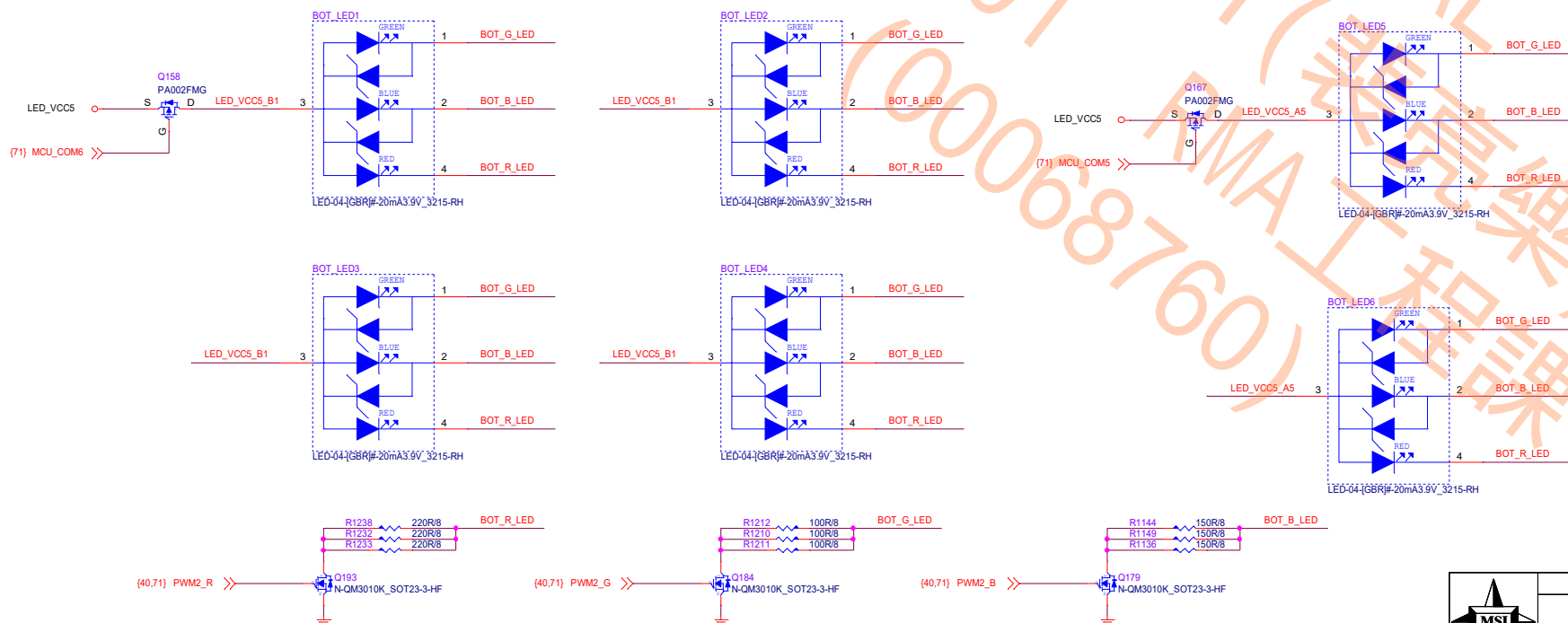
Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

DIMM_SLOT

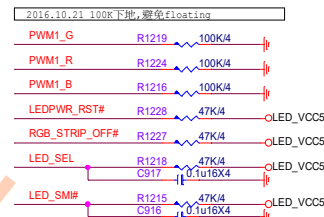
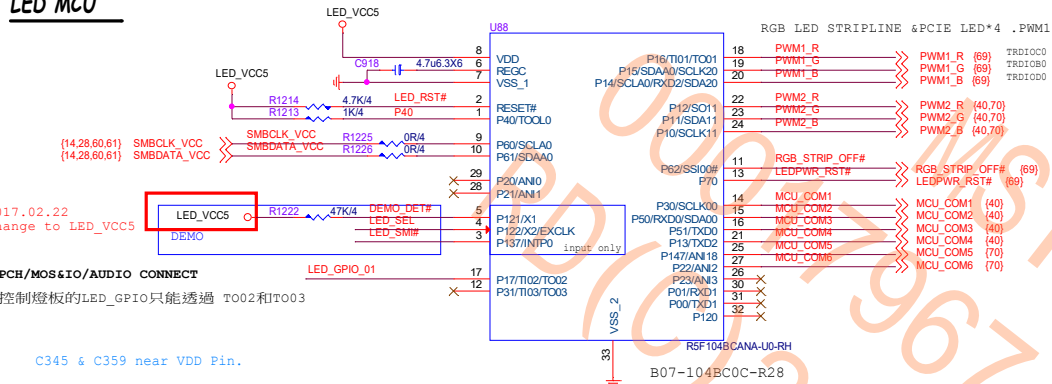
DIMM_LED >> (default) :D0C-040P100-H91



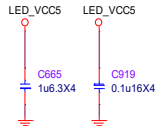
Left Trvsk LED



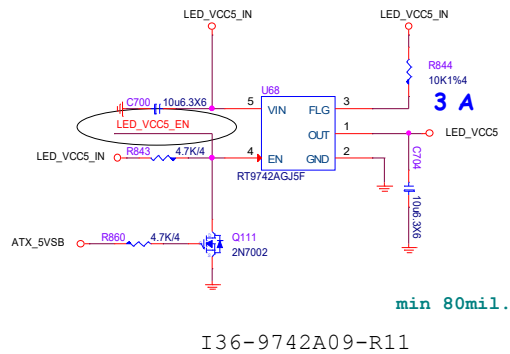
LED MCU



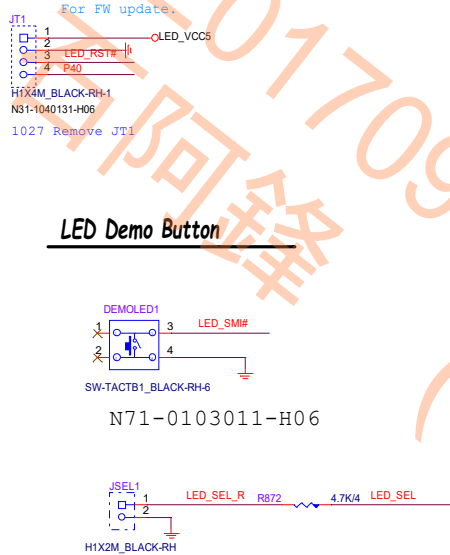
C345 & C359 near VDD Pin.



EXTERNAL POWER INPUT

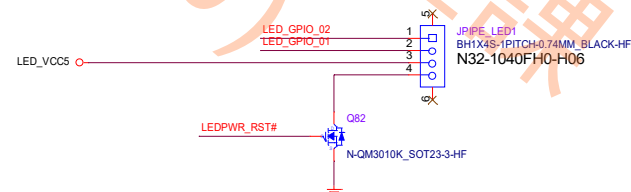


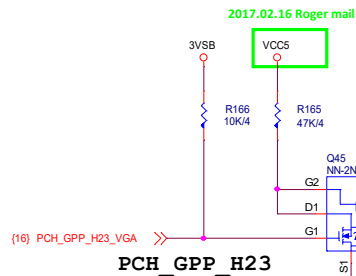
LED Demo Button



3 AUDIO/IO Cover LED

PCS LED*0.16W=W

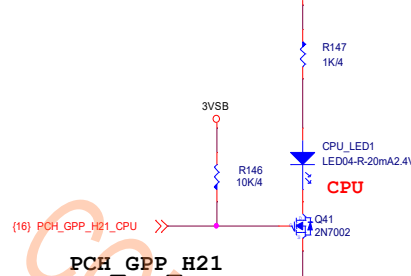
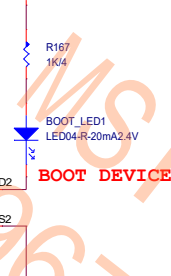
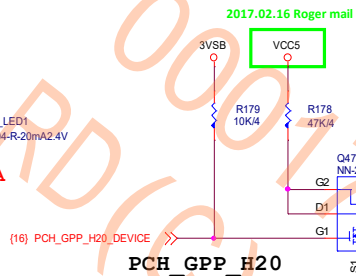




LED
紅 : D0C-040P100-H91
AVL: D0C-040S500-E07

LED
白 : D0C-040T200-H91
AVL: D0C-040S200-E07

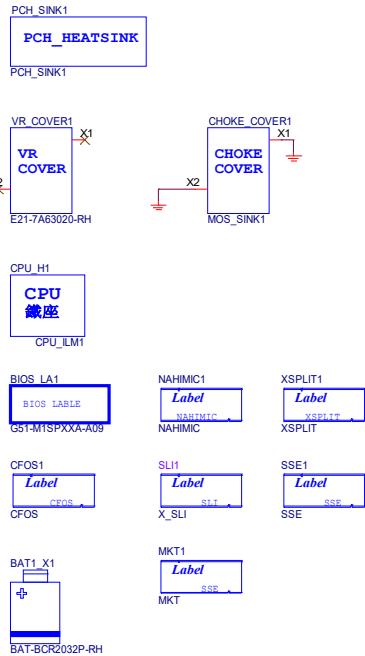
GPIO LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)



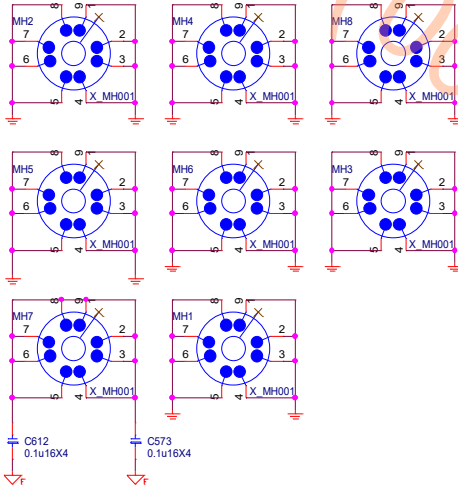
關機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU check CPU LED 亮，check PASS後則CPU LED減掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。
4. BOOT DEVICE的check/BOOT LED亮，check PASS後則BOOT LED減掉。
5. 因此最後正常順利開機後，四個LED燈都是減掉的。
(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

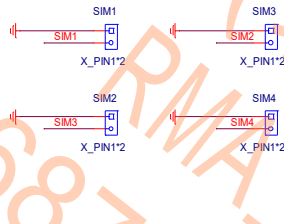
HEATSINK



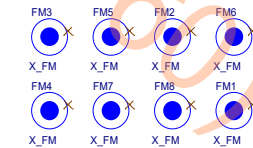
Mounting Holes



Simulation



Optical Fiducial Marks-120



Test point

